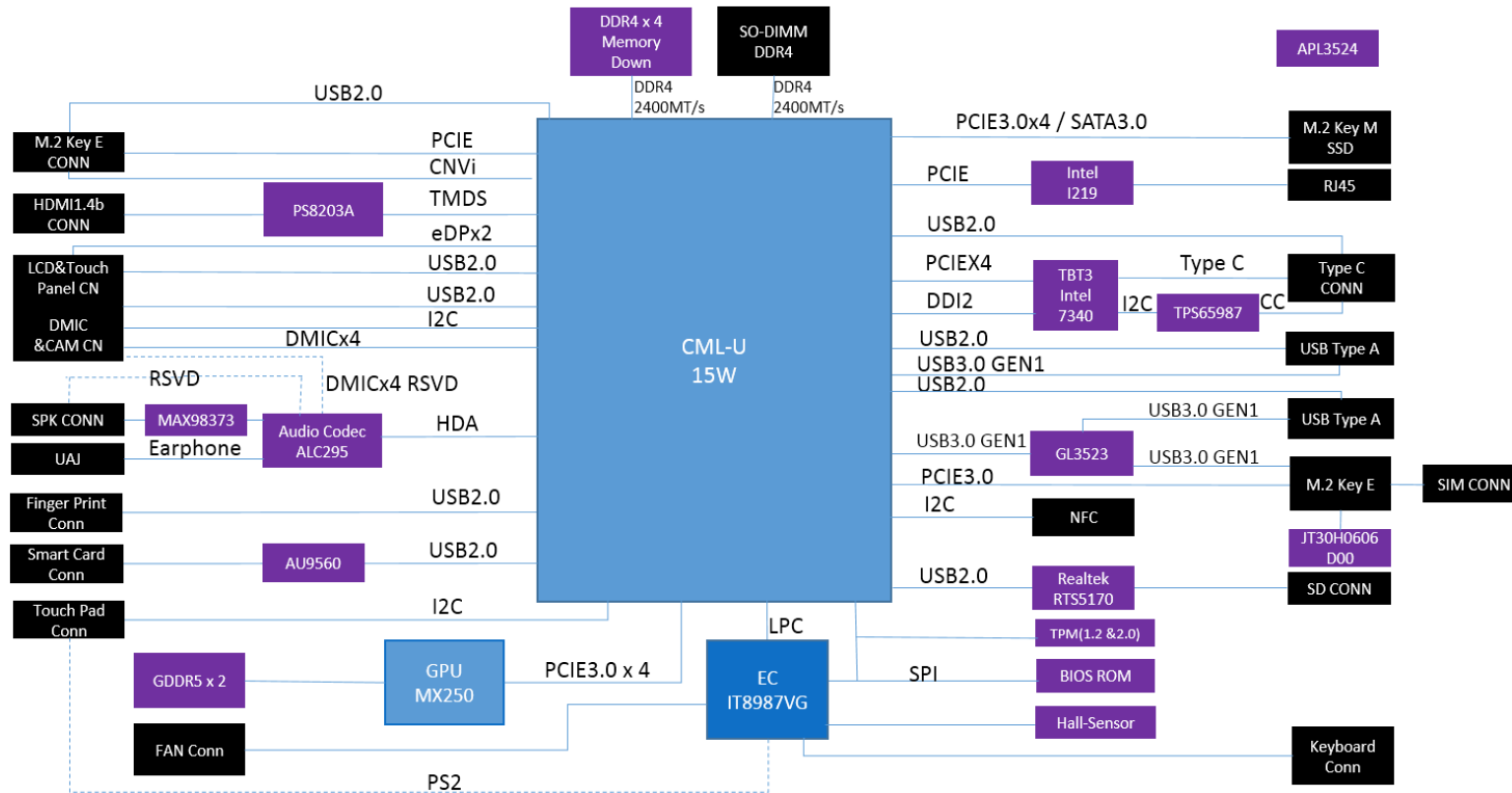
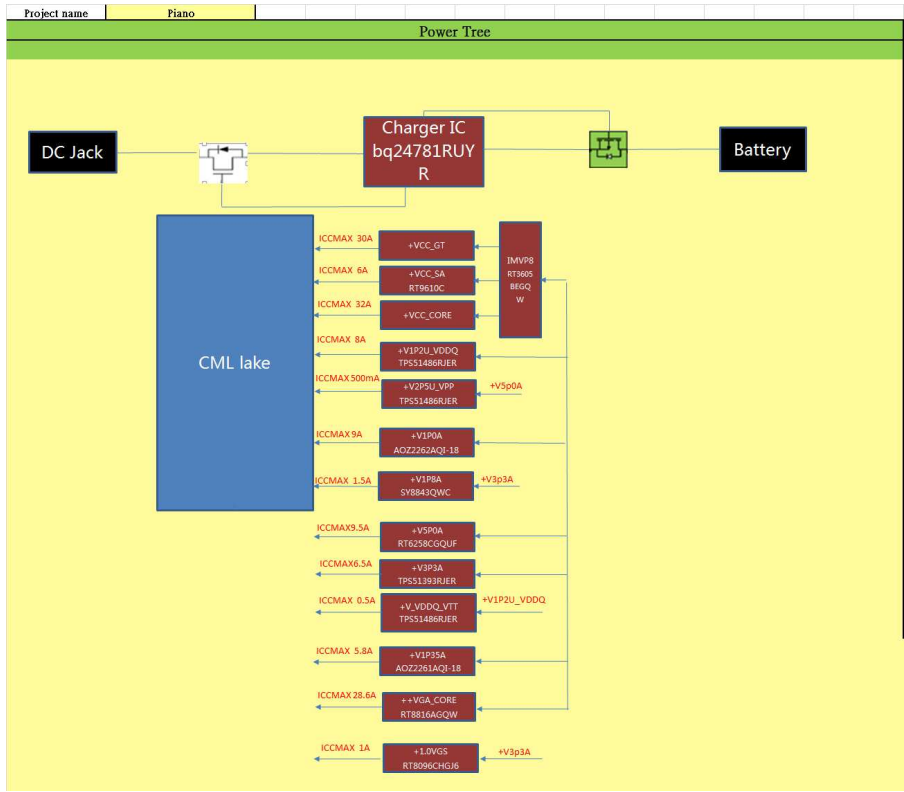


EE MB Block Diagram



3



Proj_ID	SMC_ID
Proj_ID	SMC_ID
Proj_ID	SMC_ID
Proj_ID	SMC_ID

Phase ID	PVT_001
Phase ID	PVT_001
Phase ID	PVT_001
Phase ID	PVT_001

MEM ID	MEM_ID1	MEM_ID2	MEM_ID3	MEM_ID4	MEM_ID5
MEM_ID	MEM_ID1	MEM_ID2	MEM_ID3	MEM_ID4	MEM_ID5
MEM_ID	MEM_ID1	MEM_ID2	MEM_ID3	MEM_ID4	MEM_ID5
MEM_ID	MEM_ID1	MEM_ID2	MEM_ID3	MEM_ID4	MEM_ID5

GPIO ID	GPIO_ID1	GPIO_ID2
GPIO_ID	GPIO_ID1	GPIO_ID2
GPIO_ID	GPIO_ID1	GPIO_ID2
GPIO_ID	GPIO_ID1	GPIO_ID2

NFC ID	NFC_ID1	NFC_ID2
NFC_ID	NFC_ID1	NFC_ID2
NFC_ID	NFC_ID1	NFC_ID2
NFC_ID	NFC_ID1	NFC_ID2

CAM ID	CAM_ID1	CAM_ID2
CAM_ID	CAM_ID1	CAM_ID2
CAM_ID	CAM_ID1	CAM_ID2
CAM_ID	CAM_ID1	CAM_ID2

LTE ID	LTE_ID1	LTE_ID2
LTE_ID	LTE_ID1	LTE_ID2
LTE_ID	LTE_ID1	LTE_ID2
LTE_ID	LTE_ID1	LTE_ID2

UMASDGPU	UMASDGPU_ID1	UMASDGPU_ID2
UMASDGPU	UMASDGPU_ID1	UMASDGPU_ID2
UMASDGPU	UMASDGPU_ID1	UMASDGPU_ID2
UMASDGPU	UMASDGPU_ID1	UMASDGPU_ID2

CML-noVpro & CML-Vpro

CML ID	CML_ID1	CML_ID2
CML_ID	CML_ID1	CML_ID2
CML_ID	CML_ID1	CML_ID2
CML_ID	CML_ID1	CML_ID2

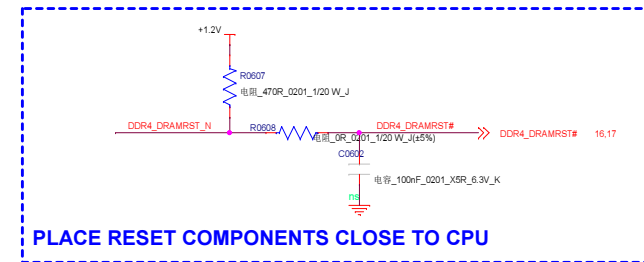
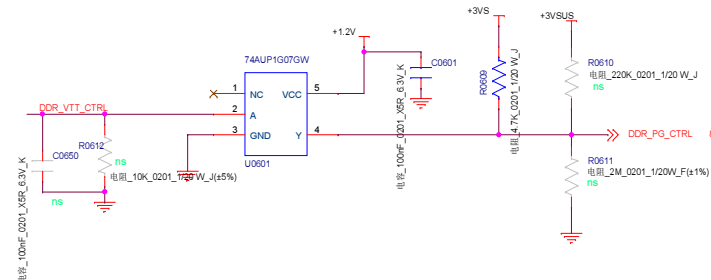
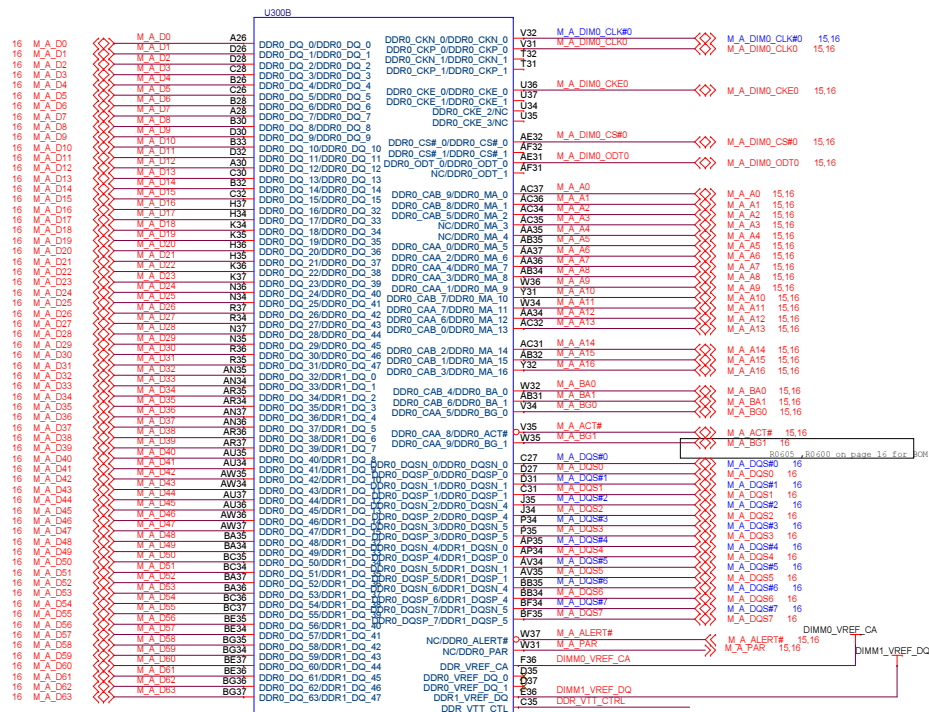
1: (DEFAULT) NORMAL OPERATION
0: LANE REVERSAL



CFG_4	0: ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1: DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT
CFG_6[6:5]	00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED 01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 2 ENABLED 10: DEVICE FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED 11: DEVICE1 FUNCTION 1, DEVICE 1 FUNCTION2 DISABLED

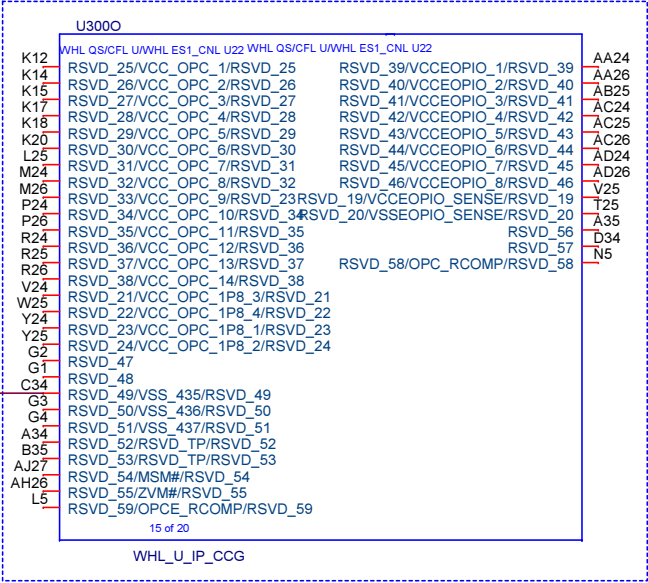
CFG_4	0: ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1: DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT
CFG_6[5]	00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED 01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED 10: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 DISABLED 11: DEVICE 1 FUNCTION 1, DEVICE 1 FUNCTION 2 DISABLED

CHA_SODIMM



BOM NOTE

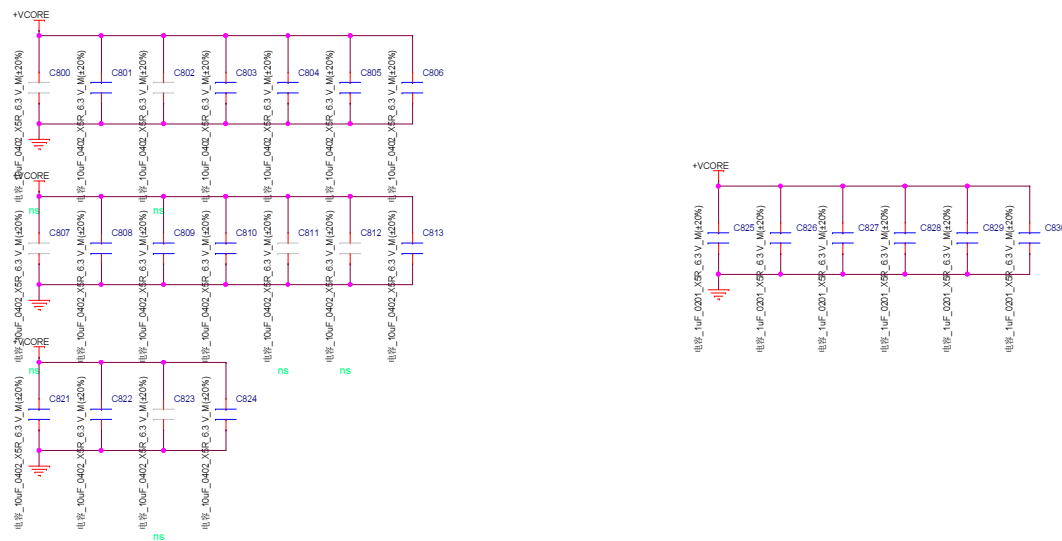
CFL-U43e/WHLU42/CMLU
[0]:121
[1]:80.6
[2]:100
CNL-U22:
100/100/100

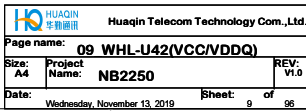


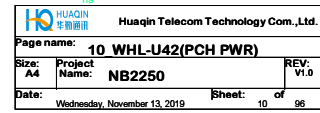
T501

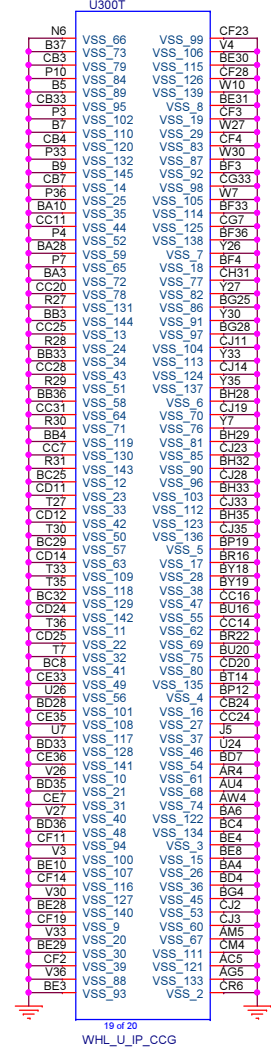
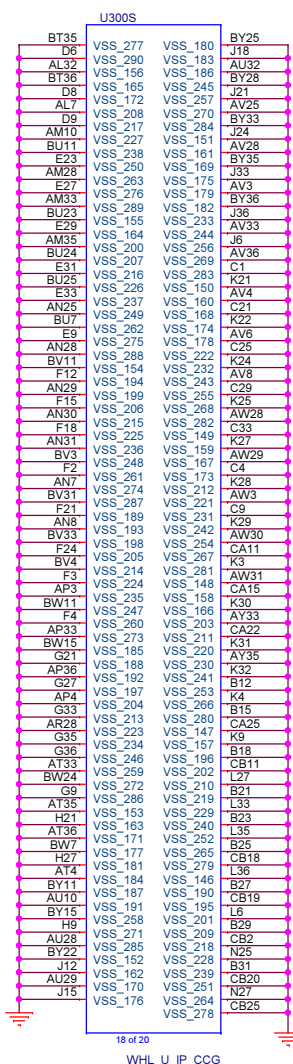
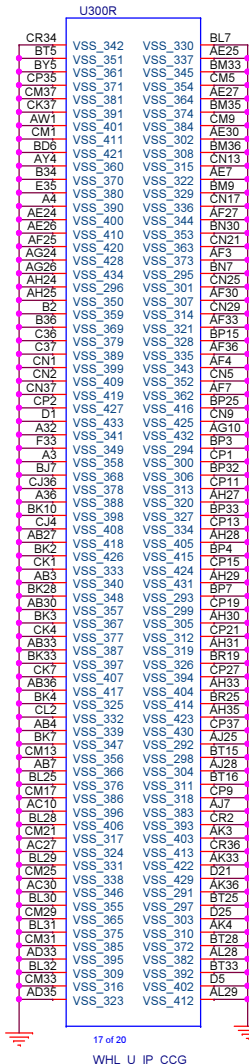
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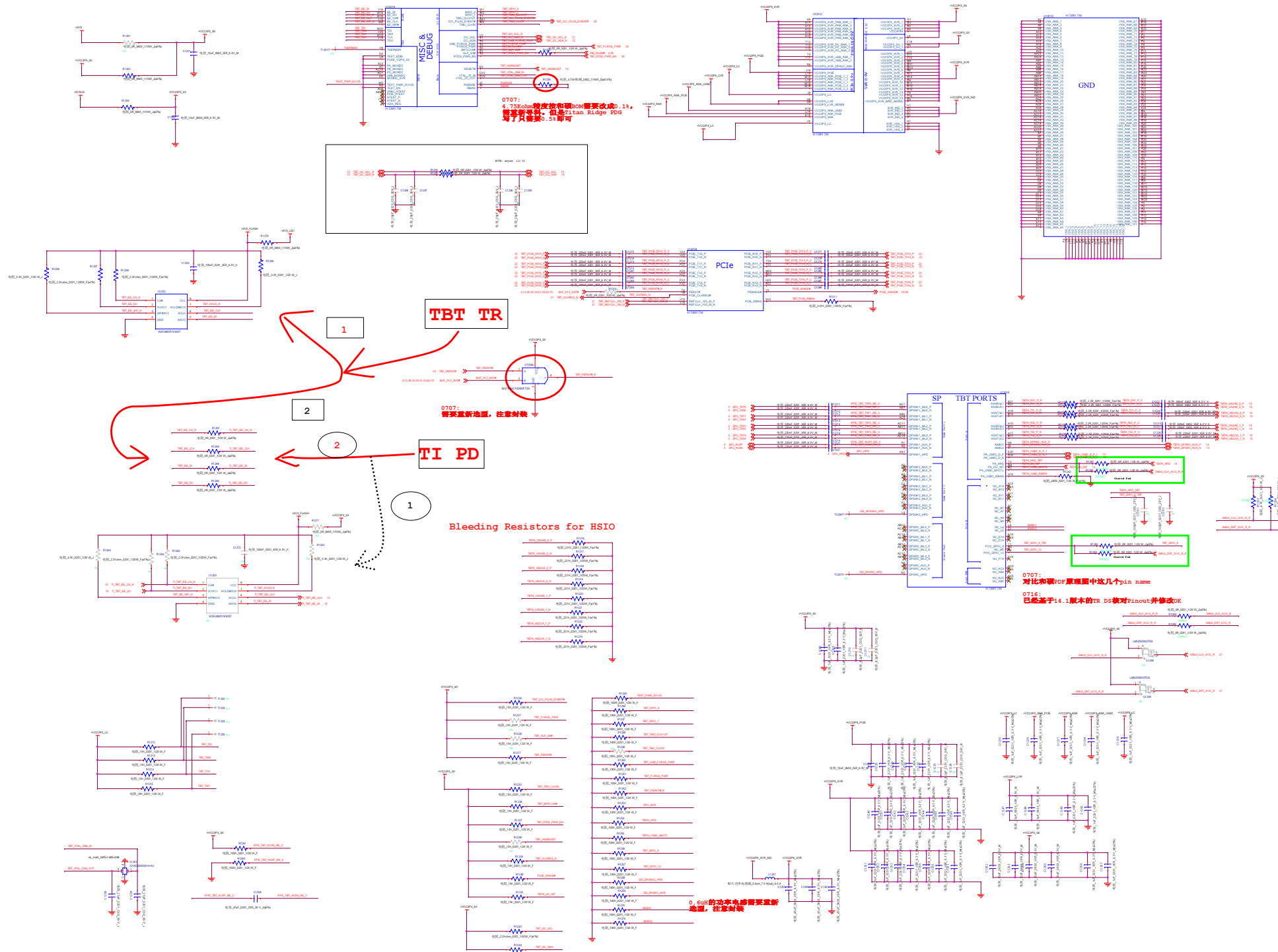
ns











0707: 需要重新布线, 注意封装
0716: 已经高于14.1版本的DS被对Pinout并修改OK

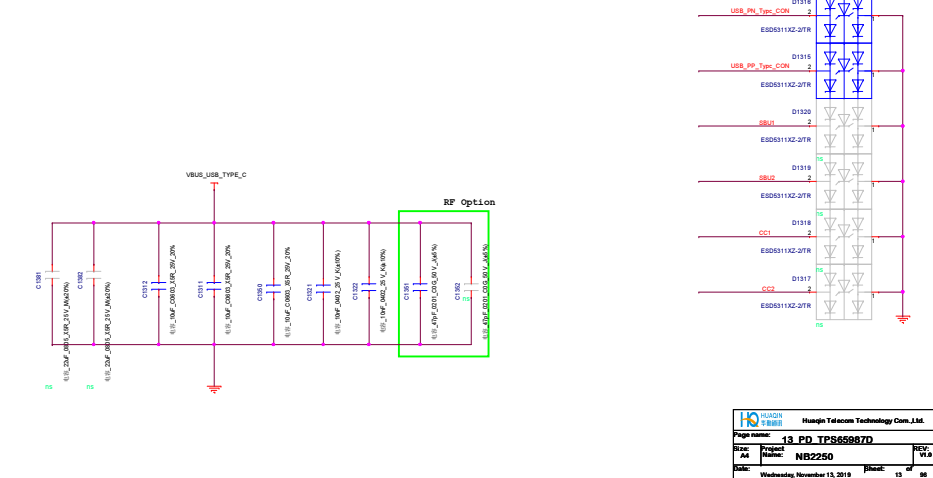
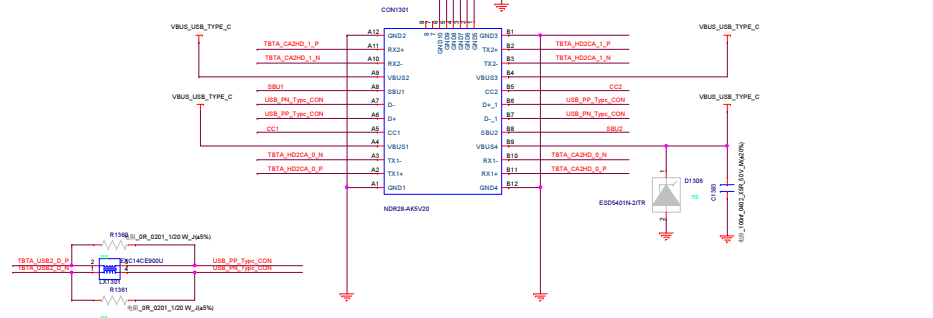
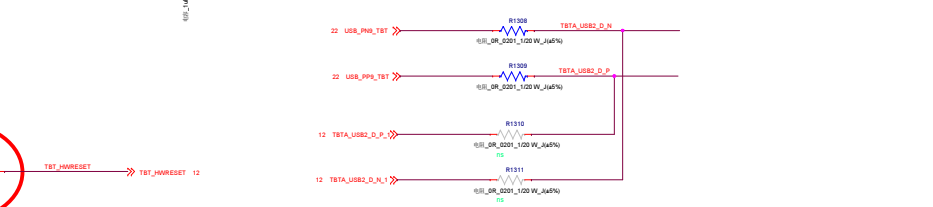
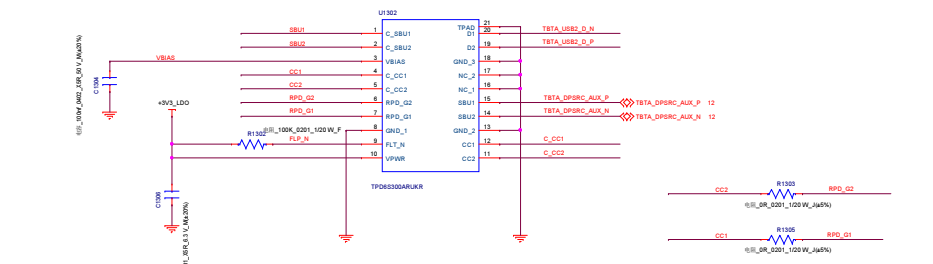
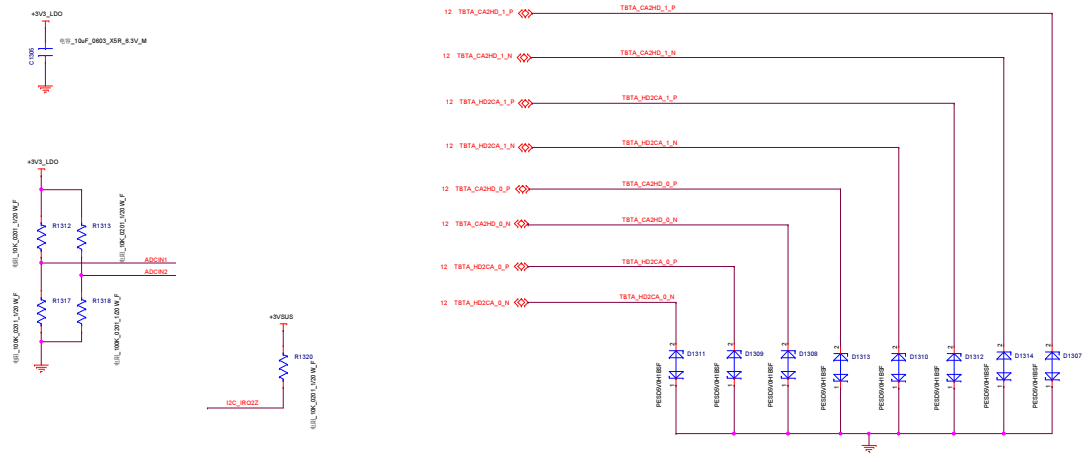
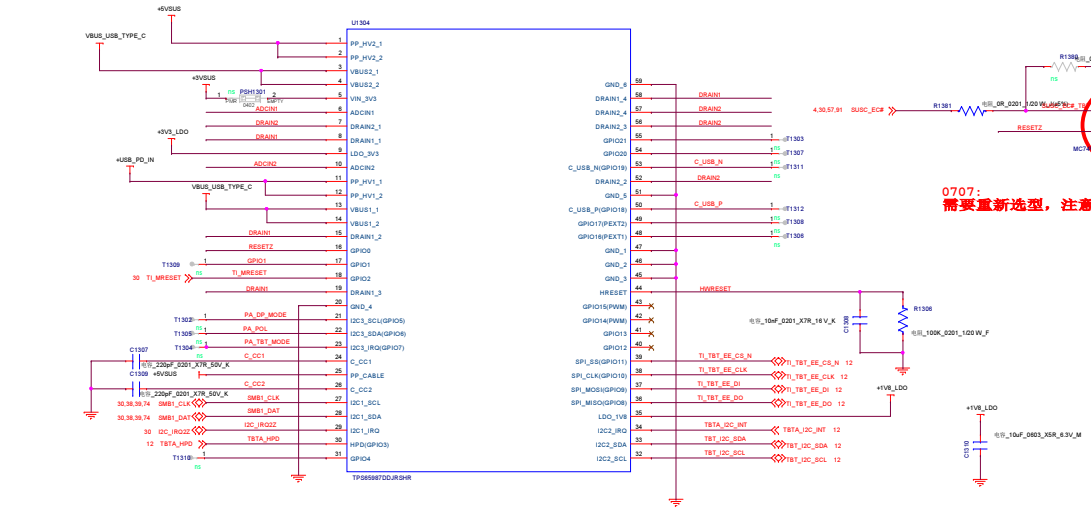
TBT TR

TI PD

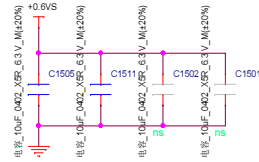
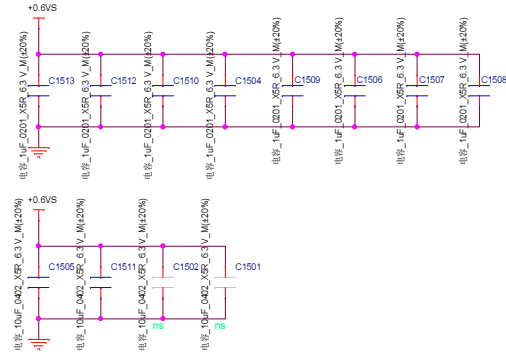
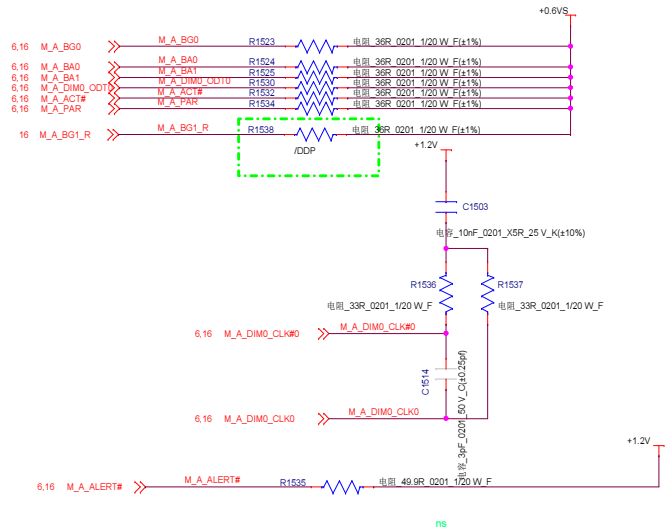
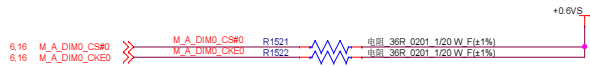
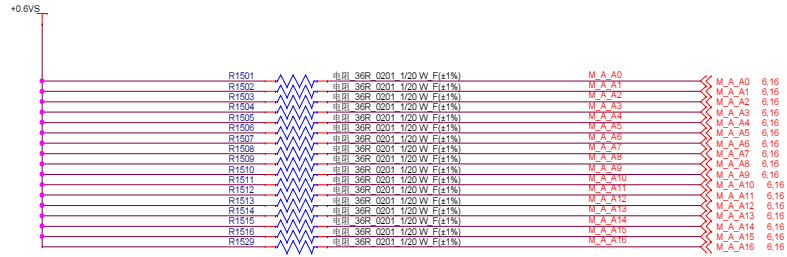
Bleeding Resistors for HSIO

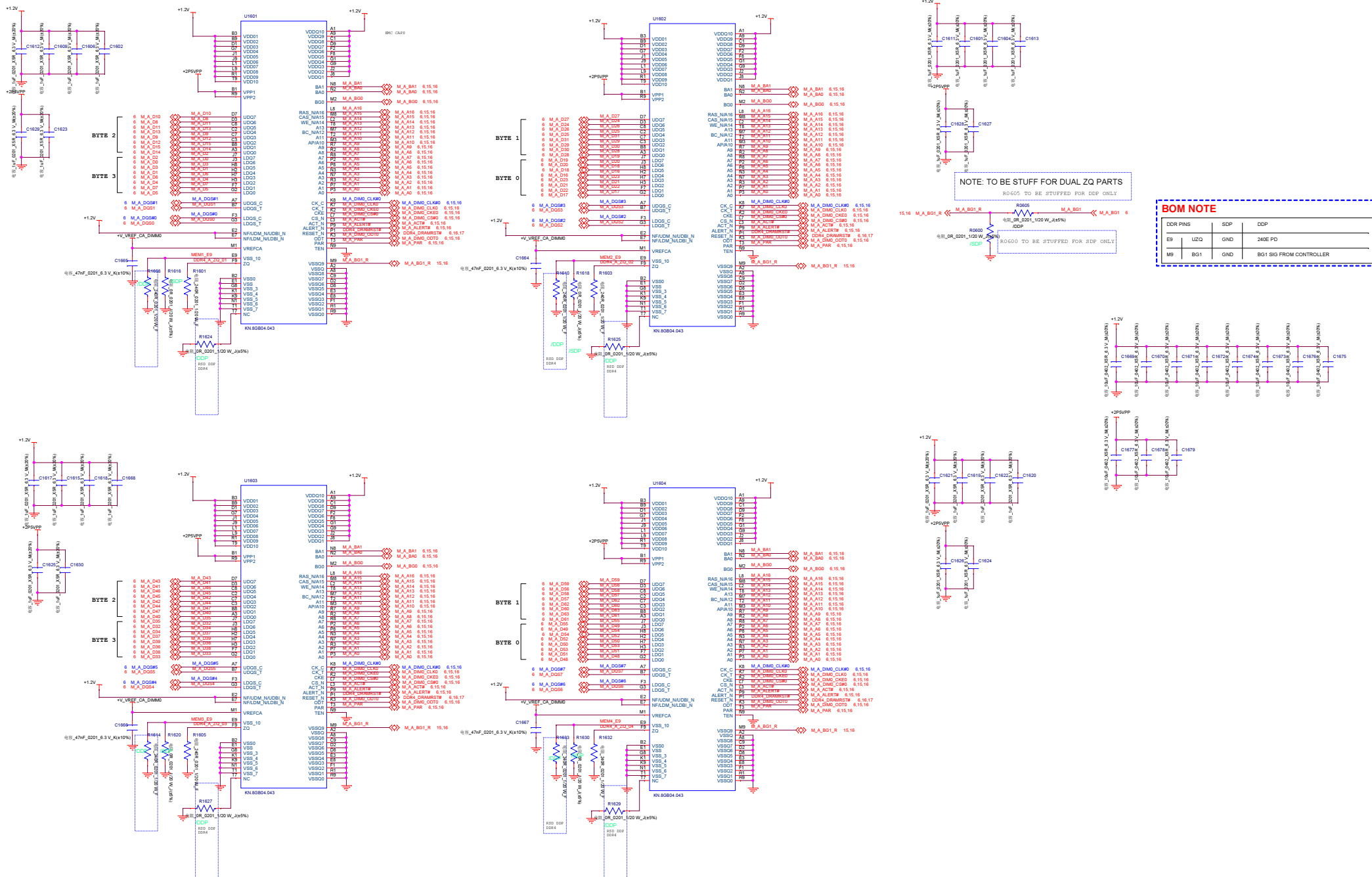
SP TBT PORTS

0707: 需要重新布线, 注意封装
0716: 已经高于14.1版本的DS被对Pinout并修改OK





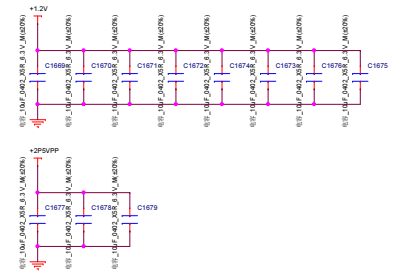


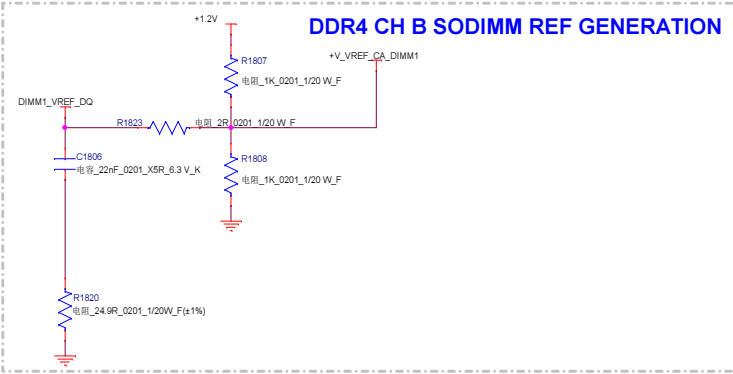
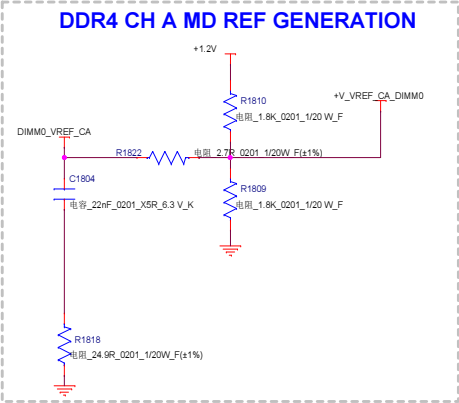


NOTE: TO BE STUFF FOR DUAL ZQ PARTS
R0605 TO BE STUFFED FOR DDP ONLY

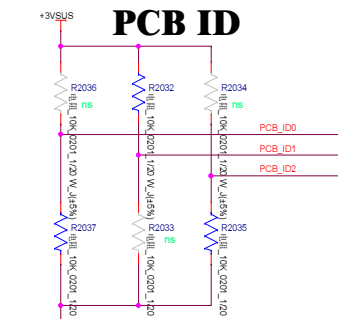
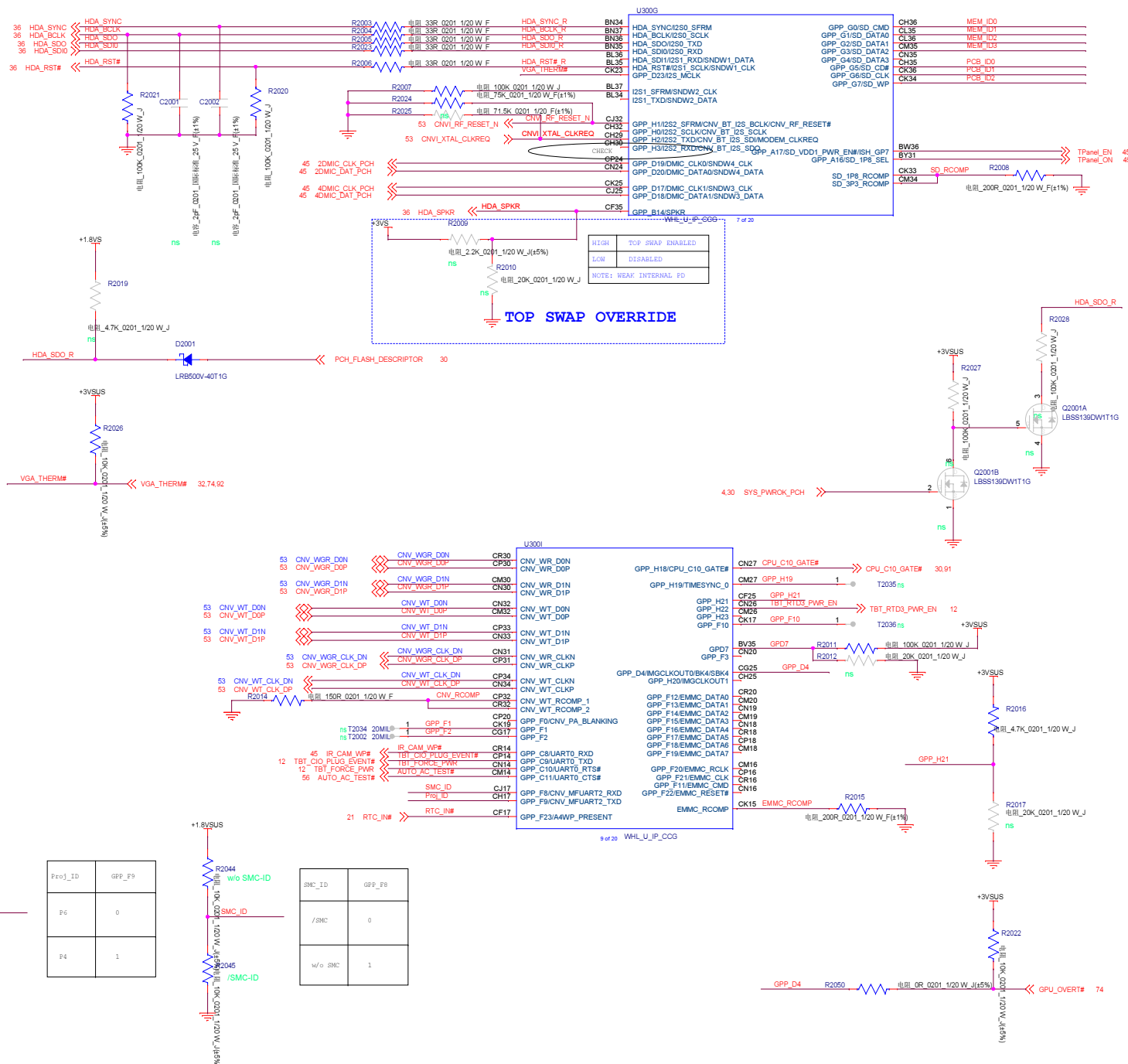
1516 M_A_B01_R ← M_A_B01_R
R0600 R0600
R0600 TO BE STUFFED FOR SDP ONLY

BOM NOTE		SDP	DDP
DDR PINS			
E9	U2Q		24DE PD
M9	BG1	GND	B01 SIG FROM CONTROLLER

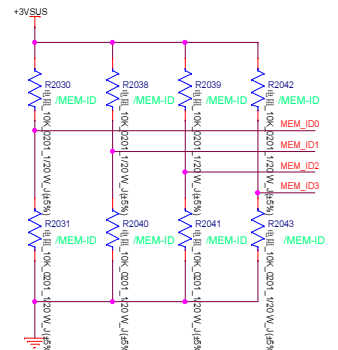




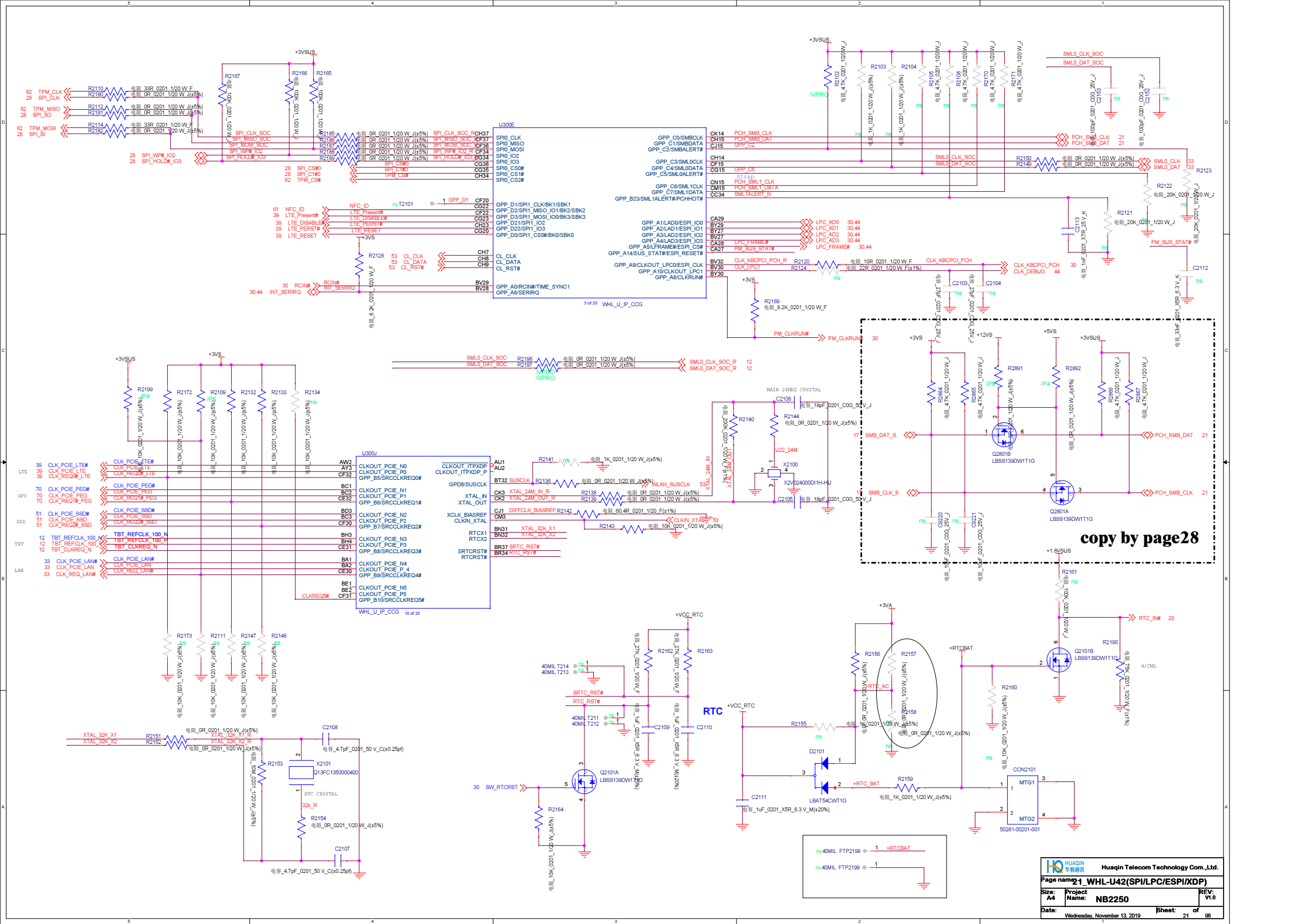


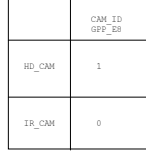
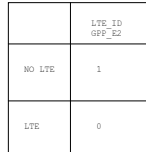
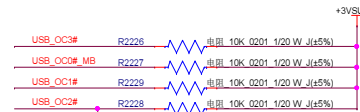


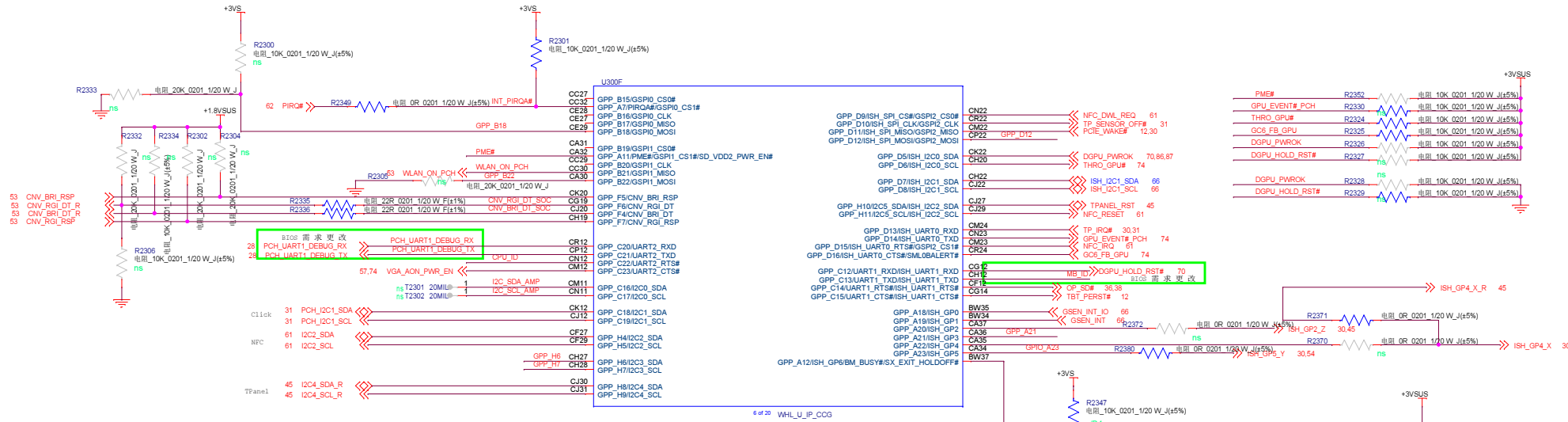
Phase	PCB_ID2 GPP_G7	PCB_ID1 GPP_G6	PCB_ID0 GPP_G5
R10	0	0	0
R11	0	0	1
R12	0	1	0
R13	0	1	1
R14	1	0	0
R15	1	0	1
R20	1	1	0



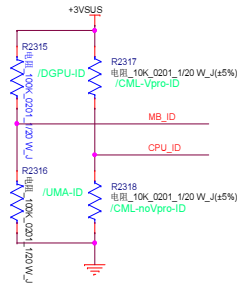
	MEM_ID3 GPP_G3	MEM_ID2 GPP_G2	MEM_ID1 GPP_G1	MEM_ID0 GPP_G0
MEMCROW MT40A1G16XN8-075:R DDR	0	0	0	0
HY6L1S H5AN866MCR-VWC DDR	0	0	0	1
HY6L1S H5AN866MCR-VWC DDR	0	0	1	0
MEMCROW MT40A512M16T8-062E:J DDR	0	1	0	0
	0	1	1	0





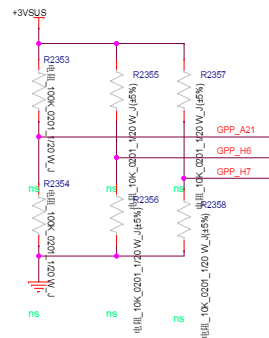


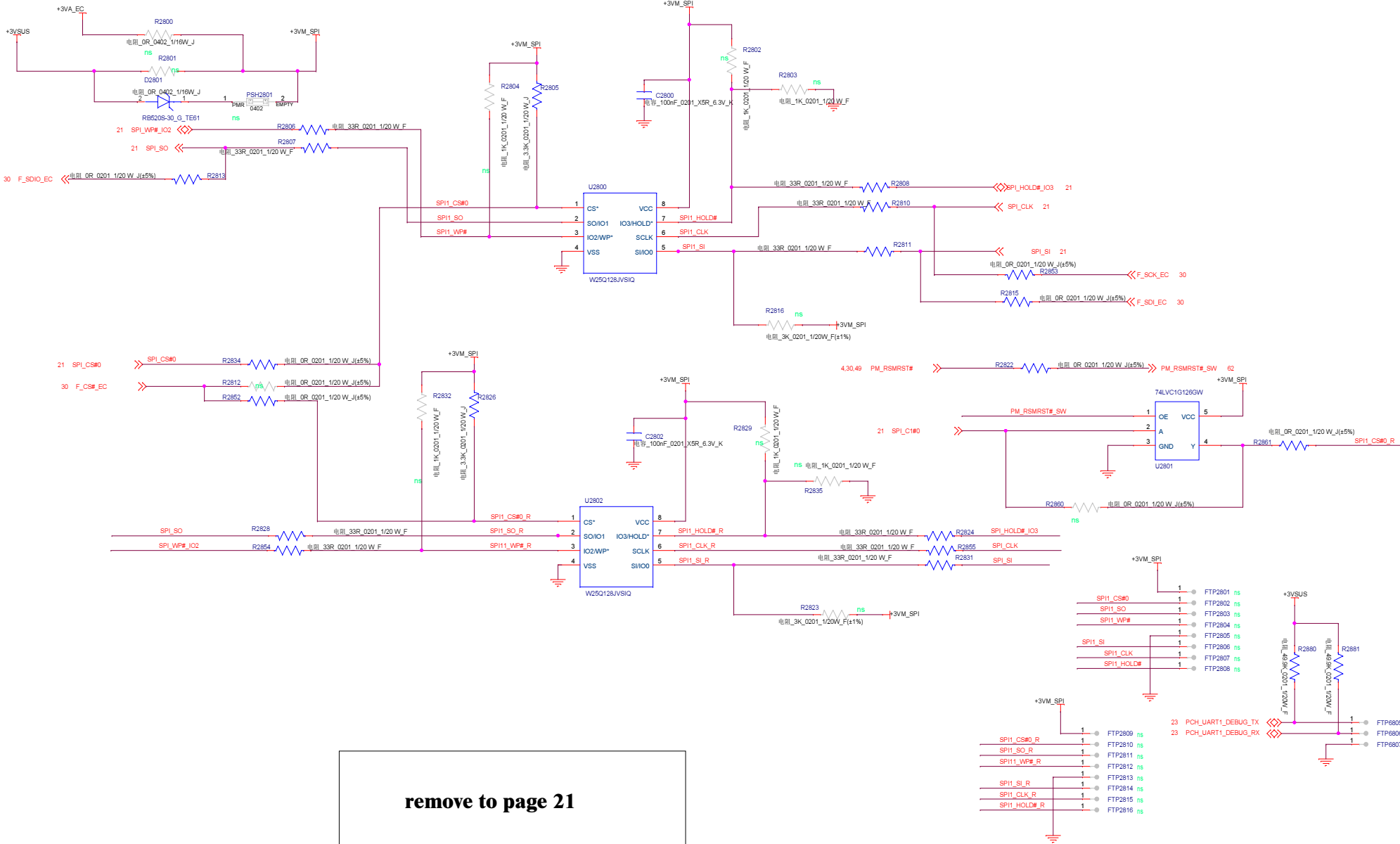
CPU BD ID



MB ID	0
UMA	0
DGPU	1

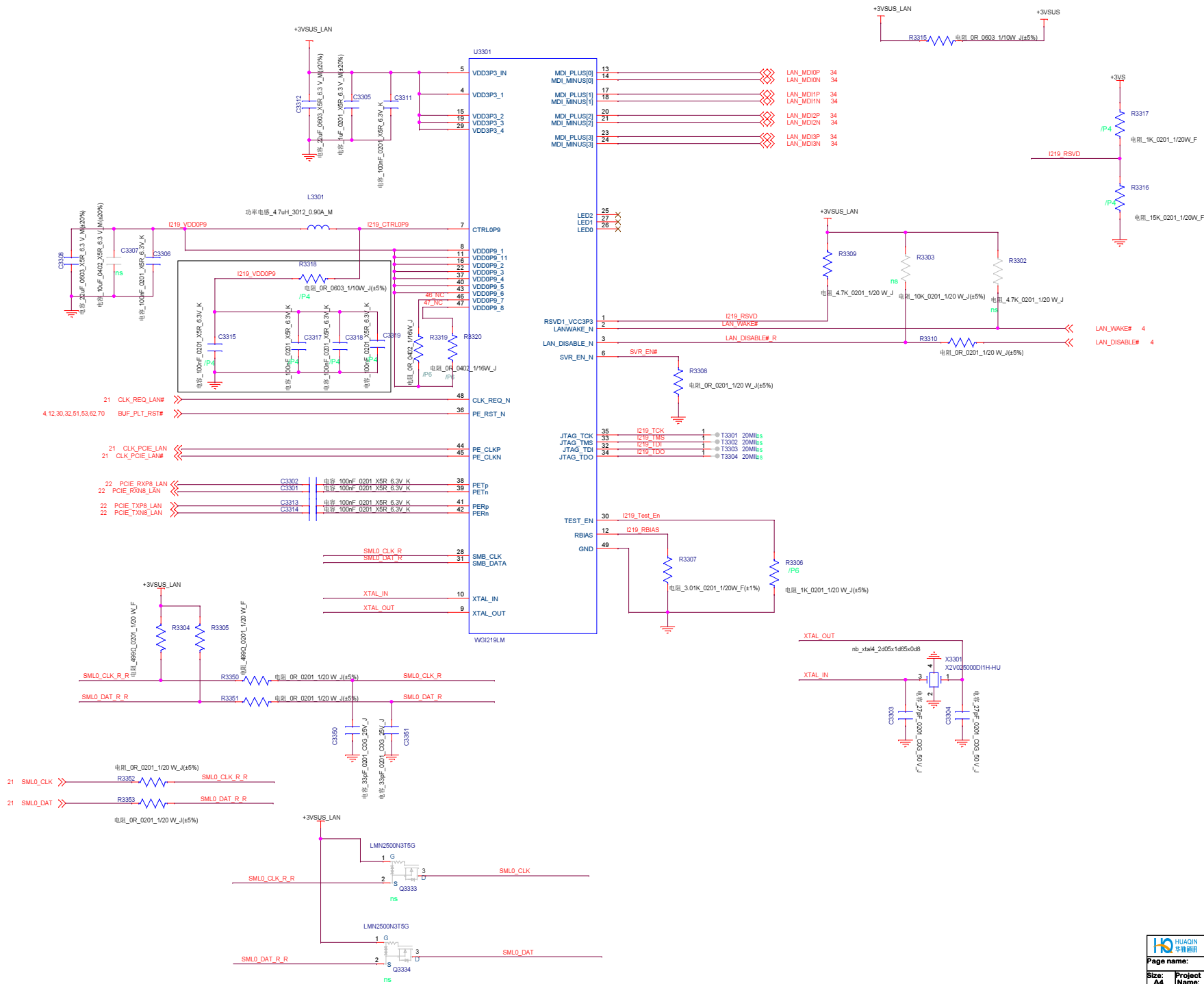
CPU ID	0
/CML-noVpro	1

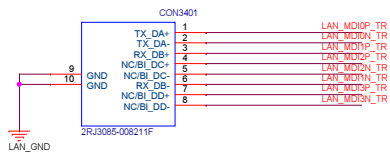
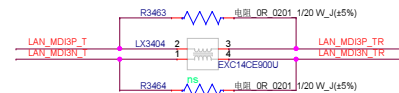
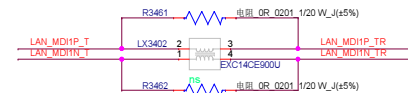
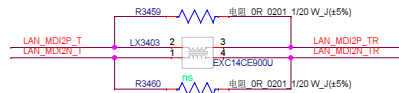
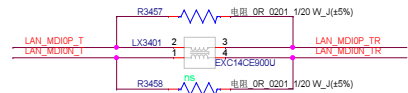
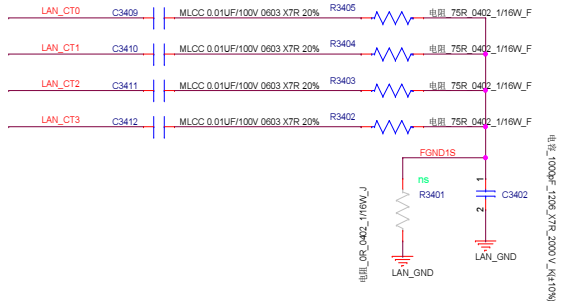
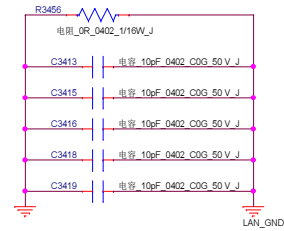
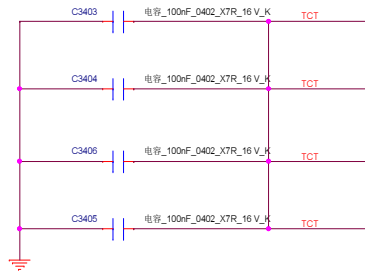
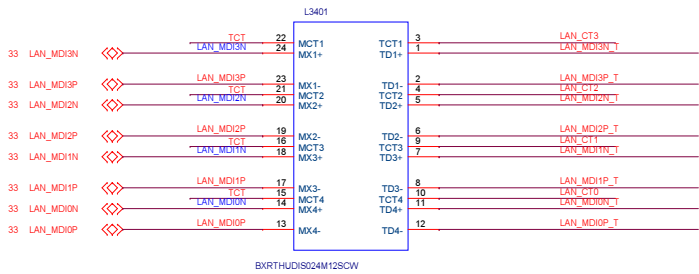




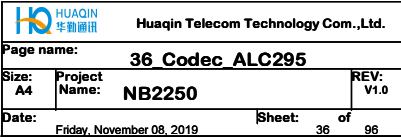
remove to page 21





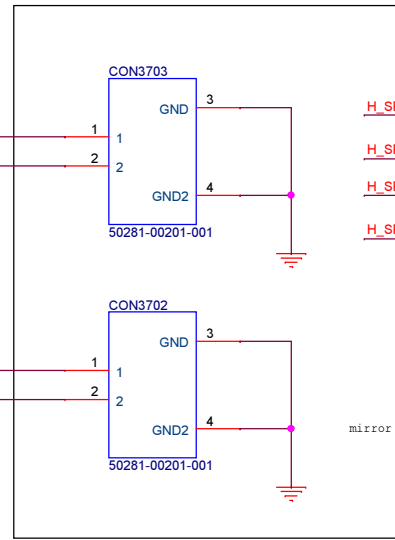
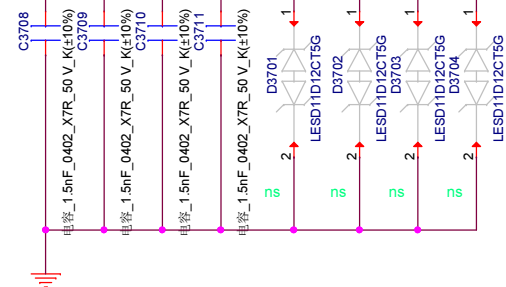






38 HDA_SPKR_LP_AMP>> R3716 电阻 0R 0402 1/16W J
38 HDA_SPKR_LN_AMP>> R3717 电阻 0R 0402 1/16W J
38 HDA_SPKR_RP_AMP>> R3718 电阻 0R 0402 1/16W J
38 HDA_SPKR_RN_AMP>> R3719 电阻 0R 0402 1/16W J

36 HDA_SPKR_LP>> R3750 电阻 0R 0402 1/16W J
36 HDA_SPKR_LN>> R3751 电阻 0R 0402 1/16W J
36 HDA_SPKR_RP>> R3752 电阻 0R 0402 1/16W J
36 HDA_SPKR_RN>> R3753 电阻 0R 0402 1/16W J



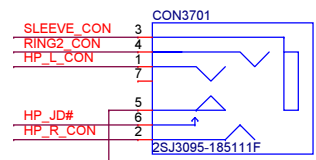
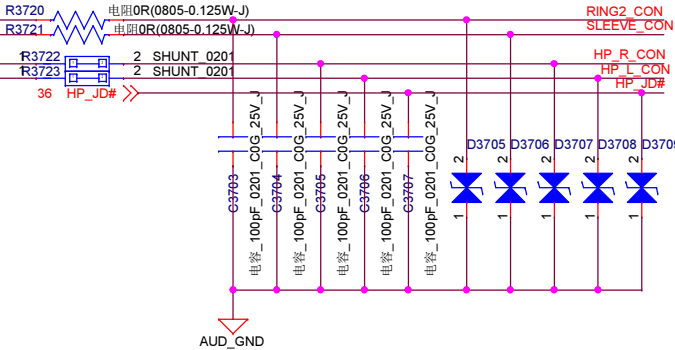
H_SPKL+_R 1 FTP3701 ns
H_SPKL-_R 1 FTP3702 ns
H_SPKR+_R 1 FTP3703 ns
H_SPKR-_R 1 FTP3704 ns

36 MIC2-VREFO-R>> R3706 电阻 2.2K 0201 1/20 W J(±5%)
36 MIC2-VREFO-L>> R3705 电阻 2.2K 0201 1/20 W J(±5%)

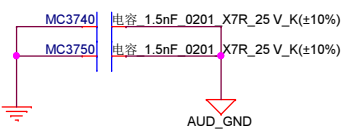
36 RING2>> R3720 电阻 0R(0805-0.125W-J)
36 SLEEVE>> R3721 电阻 0R(0805-0.125W-J)

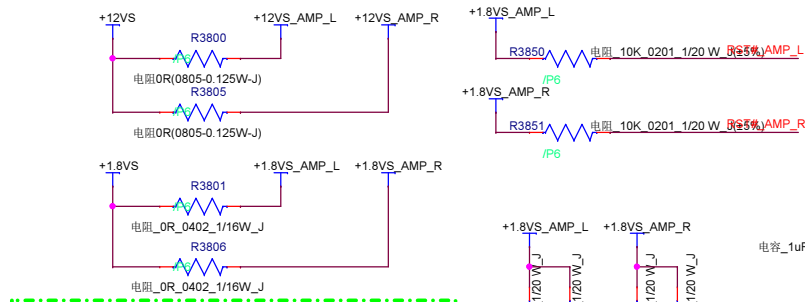
36 AC_HP_R>> 电阻 56R 0201 1/20 W J
36 AC_HP_L>> 电阻 56R 0201 1/20 W J

36 LINE1_L>> C3701 电容 4.7uF 0402 X5R 6.3 V M(±20%)
36 LINE1_R>> C3702 电容 4.7uF 0402 X5R 6.3 V M(±20%)

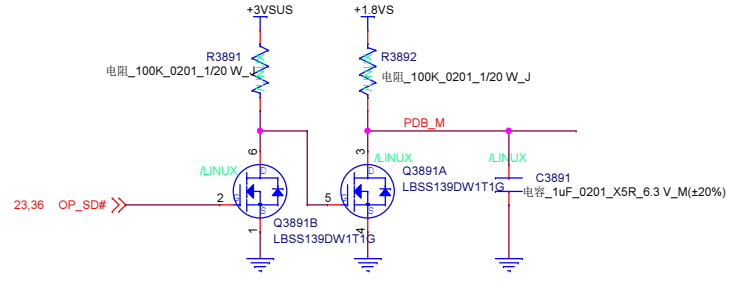
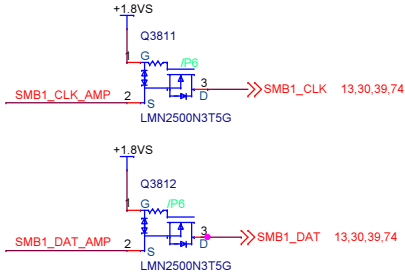
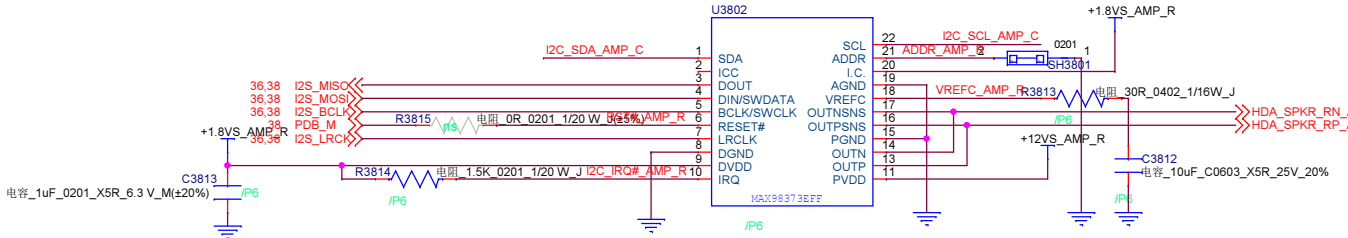
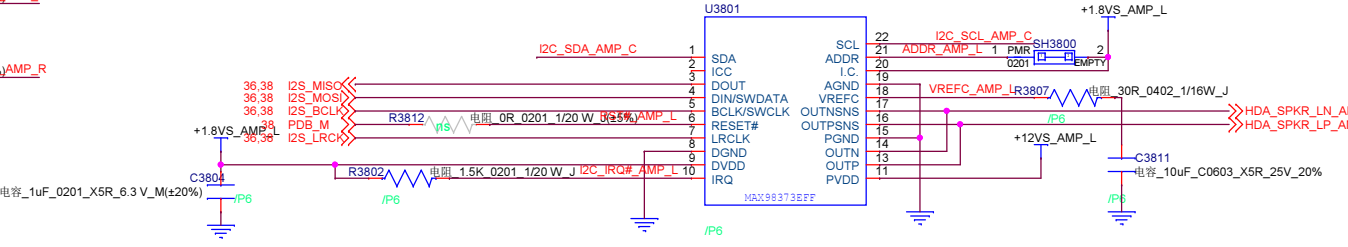
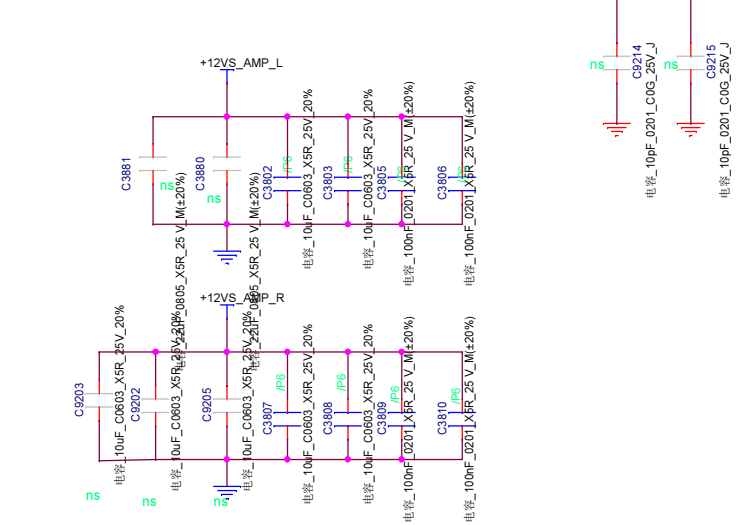


SLEEVE_CON 1 FTP3705 ns
RING2_CON 1 FTP3706 ns
HP_L_CON 1 FTP3707 ns
HP_JD# 1 FTP3708 ns
HP_R_CON 1 FTP3709 ns
HP_JD# 1 FTP3710 ns



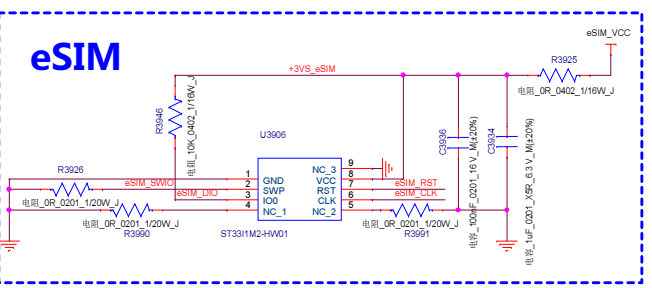
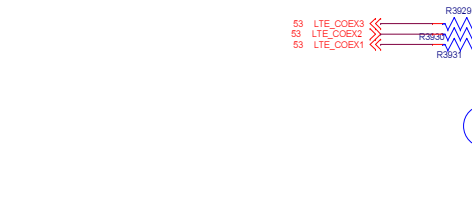
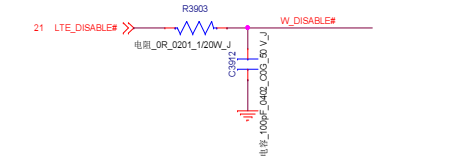
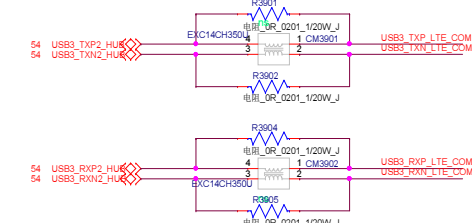
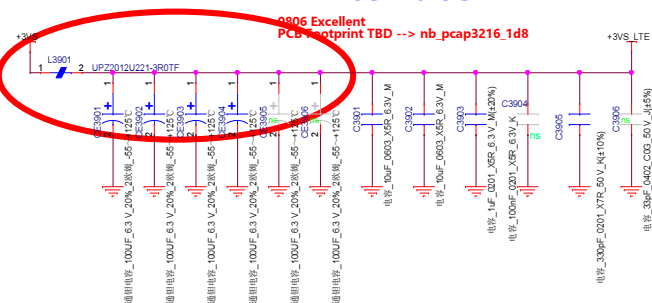


Please notice R3808, R3809, this I2C path is connected to EC for Linux. R3810, R3811, the path is connected to Codec for Windows.



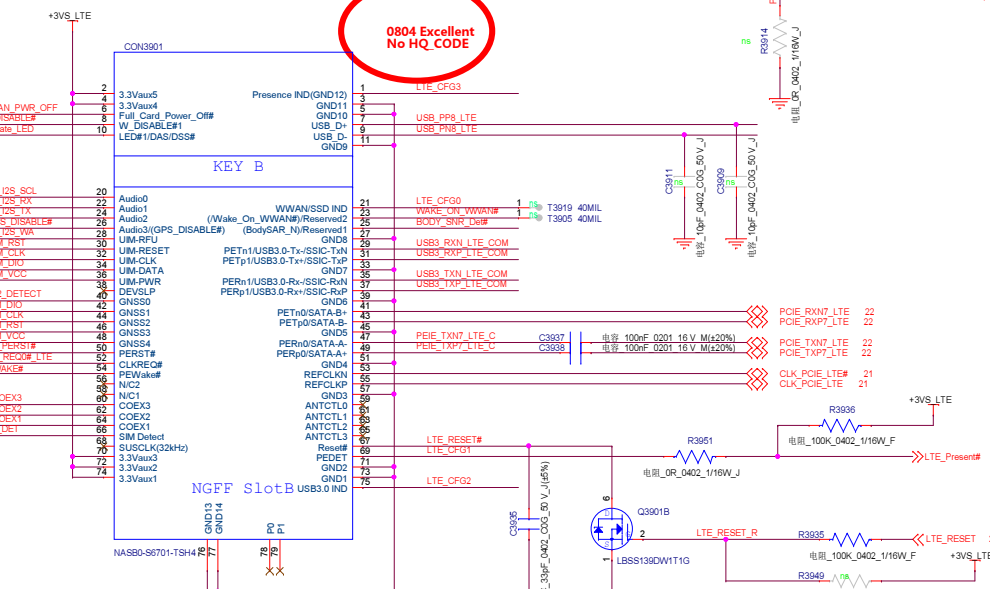
LTE Interface

8086 Excellent
PCB Footprint TBD --> nb_pcap3216_1d8

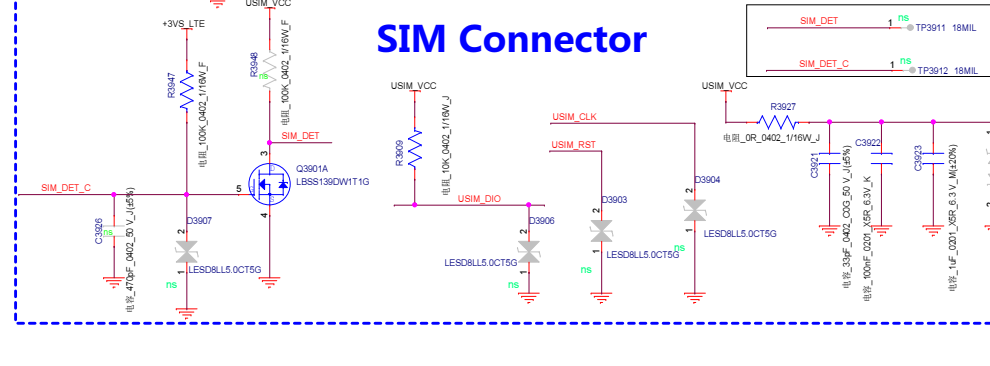


LTE Module

0804 Excellent
No HQ_CODE

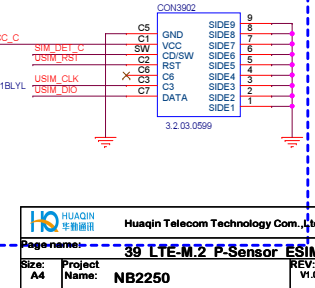
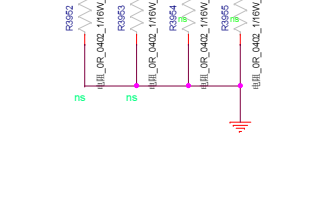
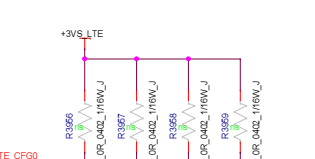
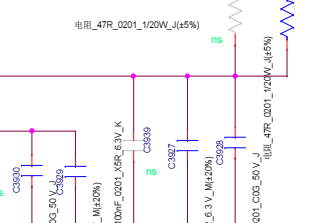
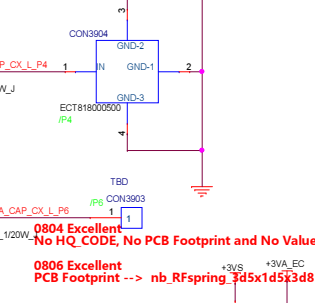


SIM Connector



LTE Interface

8086 Excellent
PCB Footprint TBD --> nb_pcap3216_1d8

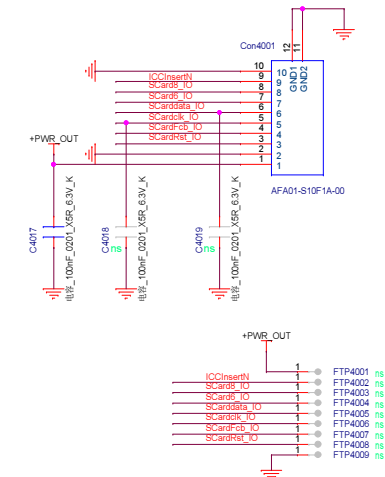
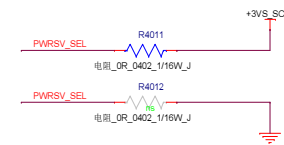


The schematic diagram illustrates the internal circuitry of the SMART CARD AU9560 module. The central component is the AU9560-GBS-GR chip, which is connected to a microcontroller (U4001) and various peripheral components. The circuit includes power management sections with +PWR_OUT, +3VS_SCR, and +5VS_SCR rails. Signal lines for Scardclk_IO and Scarddata_IO are shown, along with XT1_OUT_S and XT1_IN_S. The microcontroller (U4001) is connected to the AU9560-GBS-GR chip via a series of pins (X0 to V18OUT). The circuit also features several capacitors (C4007, C4008, C4009, C4010, C4011, C4004, C4005, C4013) and resistors (R4002, R4006, R4008, R4009, R4010, R4011) for signal conditioning and power regulation. The diagram is labeled with component values and pin numbers, providing a detailed view of the module's internal architecture.

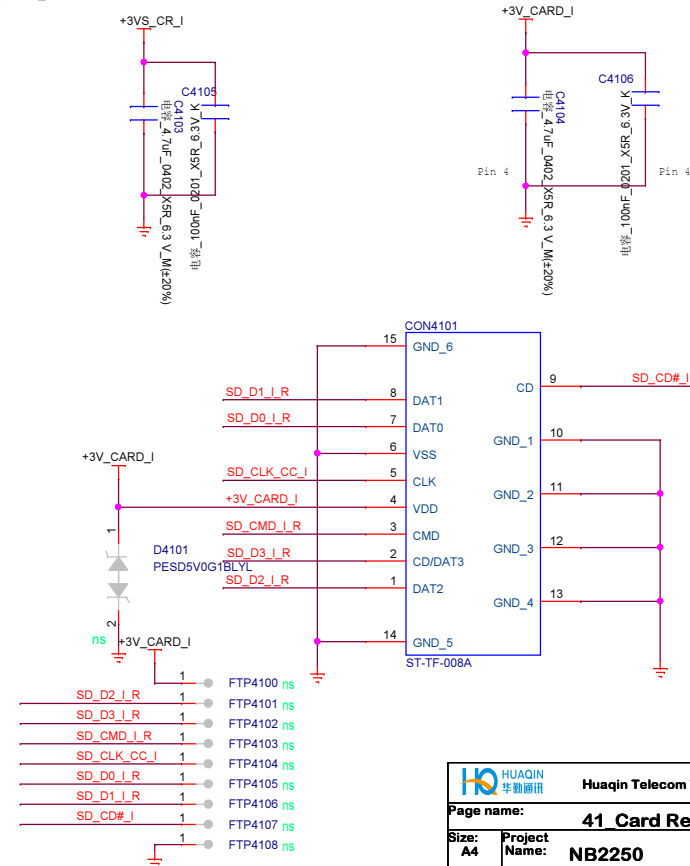
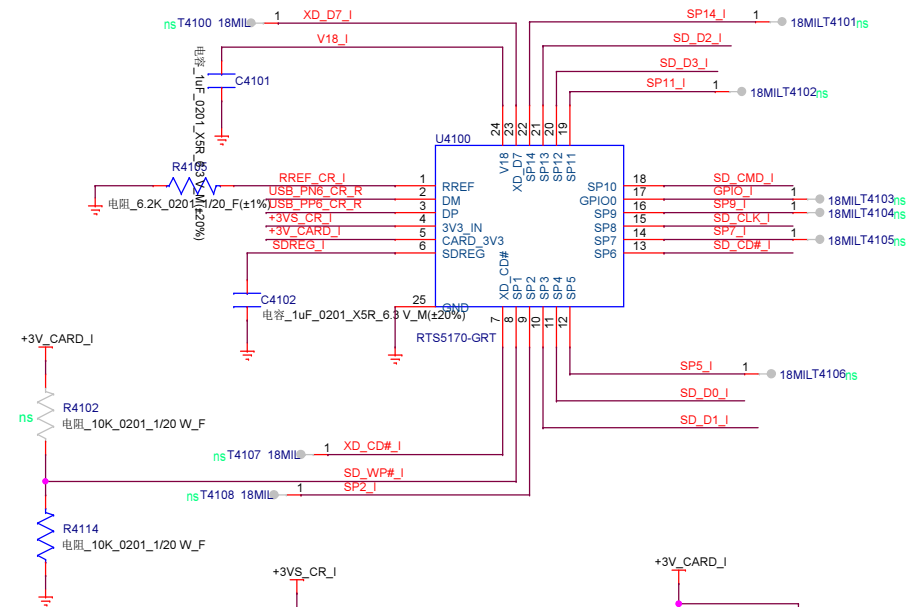
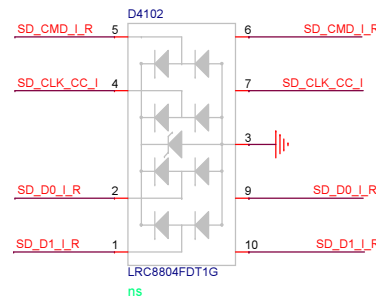
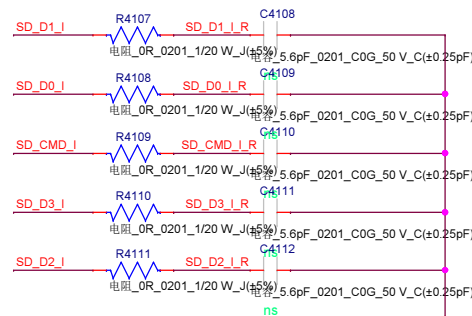
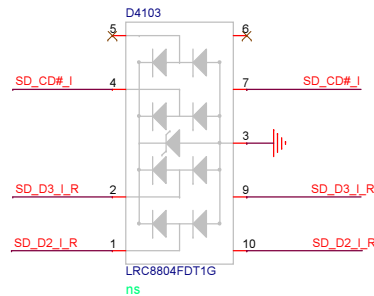
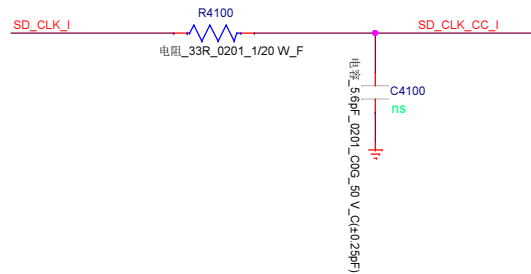
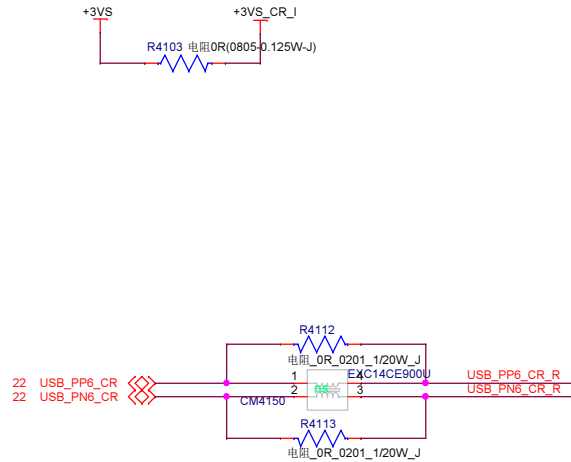
The schematic diagram illustrates the card reader interface. It features a series of components labeled D4002 through D4009, each with a PDS05V0V1BSF pinout. The connections are as follows:

- PWR_OUT** is connected to the VCC pin of all components.
- ICDInsertN** is connected to the ICDInsertN pin of all components.
- SCardData_IO** is connected to the SCardData_IO pin of all components.
- SCardS_IO** is connected to the SCardS_IO pin of all components.
- SCardB_IO** is connected to the SCardB_IO pin of all components.
- SCardFcb_IO** is connected to the SCardFcb_IO pin of all components.
- SCardRet_IO** is connected to the SCardRet_IO pin of all components.
- SCardclk_IO** is connected to the SCardclk_IO pin of all components.

The components are connected to a common ground plane, and the signal lines are routed through a series of connectors.



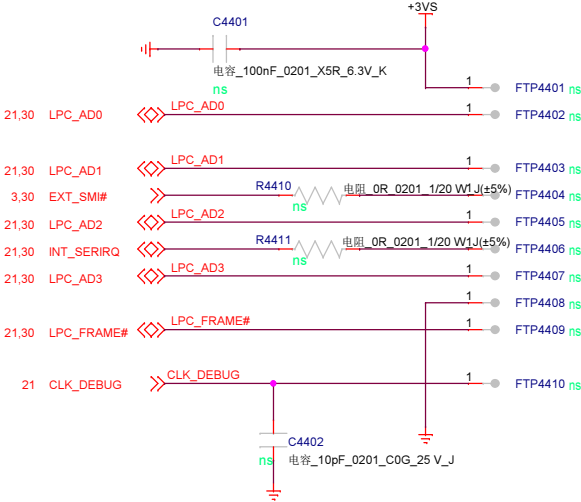
Card Reader



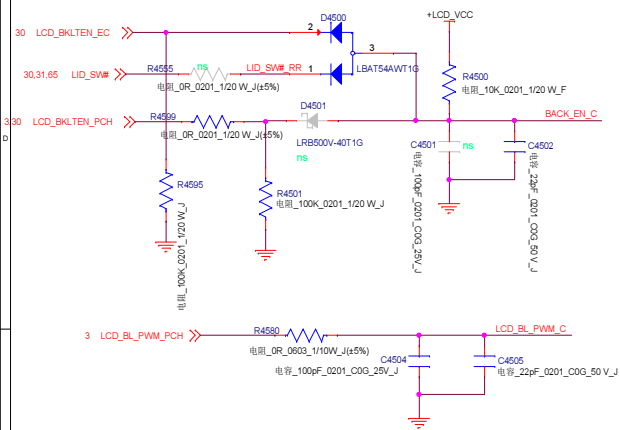




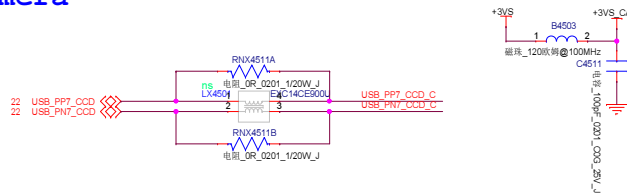
Debug



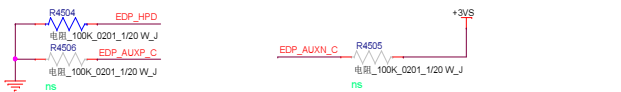
Controller circuit



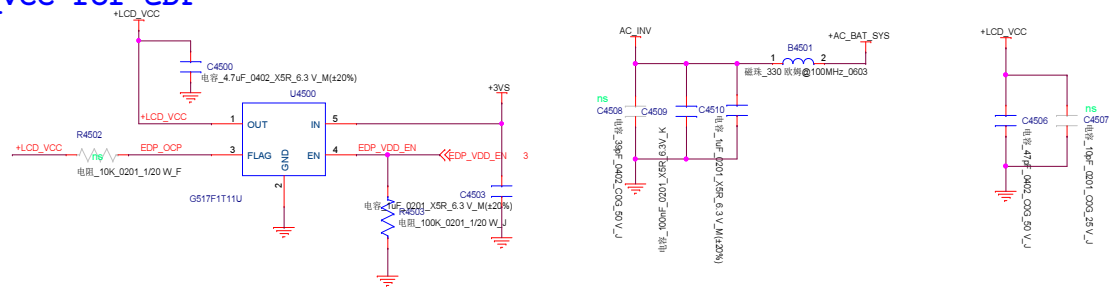
Camera



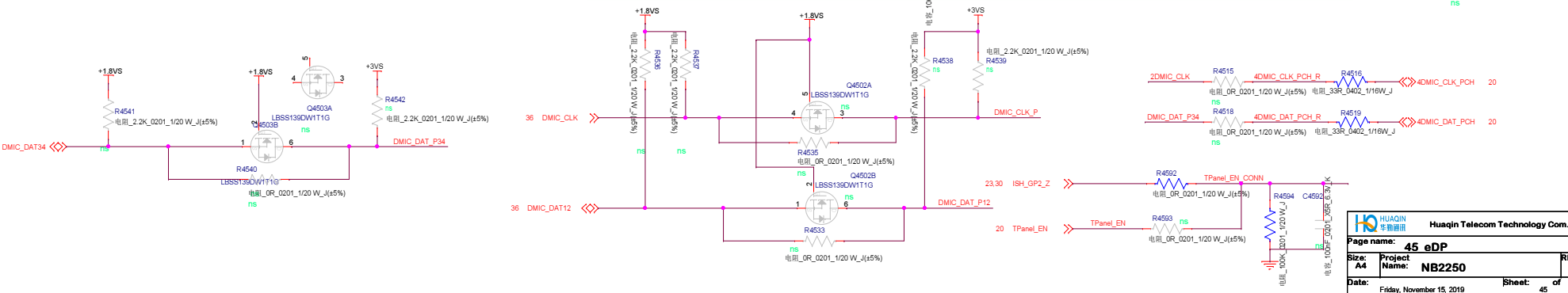
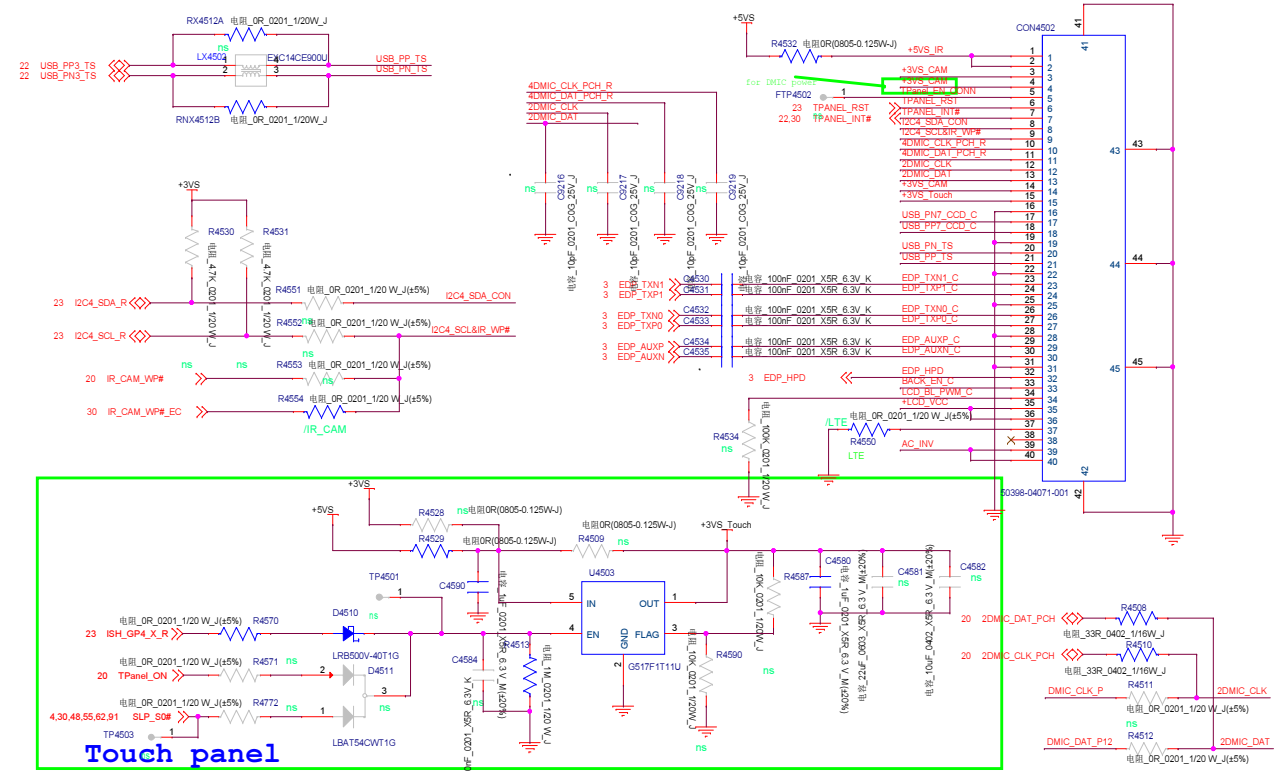
eDP HPD



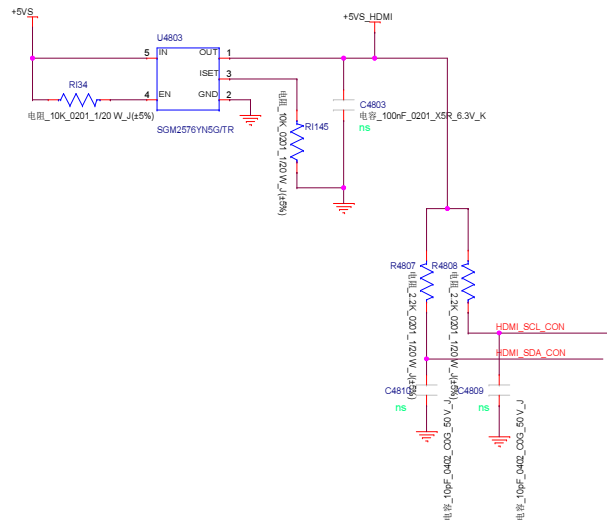
LCD_VCC for eDP



eDP CONN



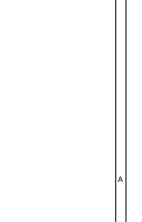
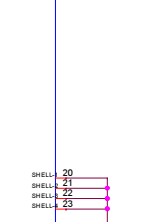
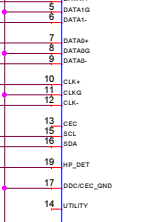
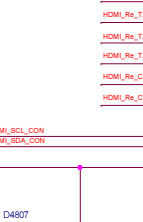
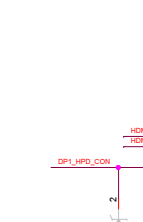
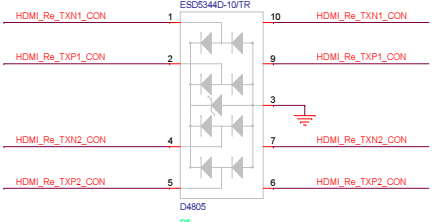
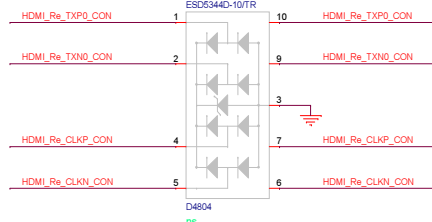
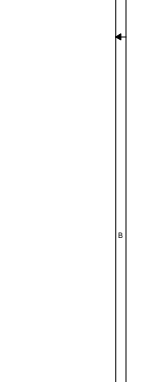
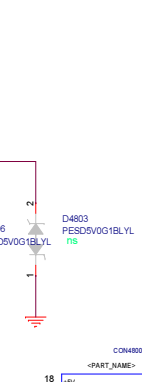
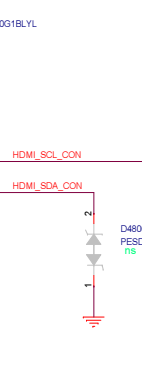
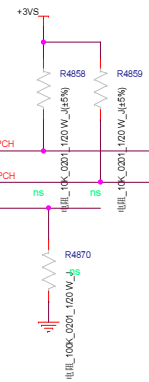
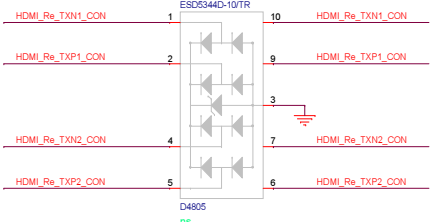
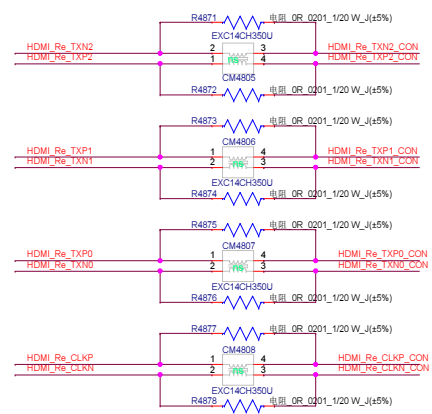
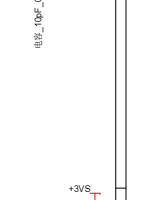
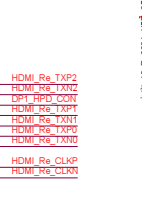
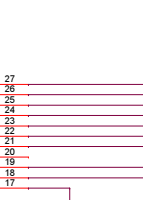
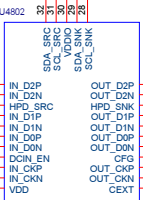
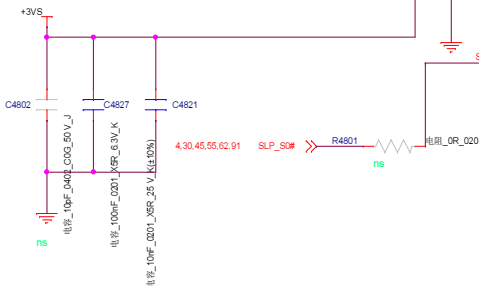
	5	4	3	2	1
D					
C					
B					
A					

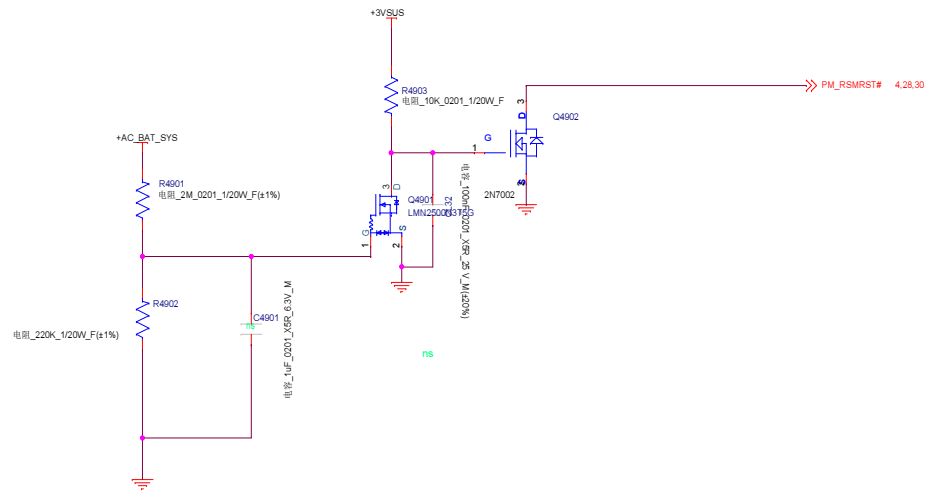


HDMI CONN

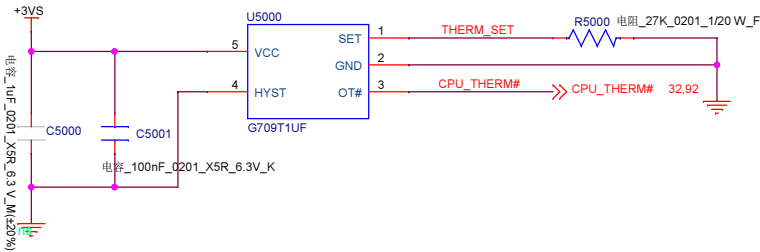
3 HDMI_TXP2
3 HDMI_TXN2
3 HDMI_TXP1
3 HDMI_TXN1
3 HDMI_TXP0
3 HDMI_TXN0
3 HDMI_CLKP
3 HDMI_CLKN

C4828 电容 100uF 0201 XSR 6.3V_K
C4829 电容 100uF 0201 XSR 6.3V_K
C4830 电容 100uF 0201 XSR 6.3V_K
C4831 电容 100uF 0201 XSR 6.3V_K
C4832 电容 100uF 0201 XSR 6.3V_K
C4833 电容 100uF 0201 XSR 6.3V_K
C4834 电容 100uF 0201 XSR 6.3V_K
C4835 电容 100uF 0201 XSR 6.3V_K

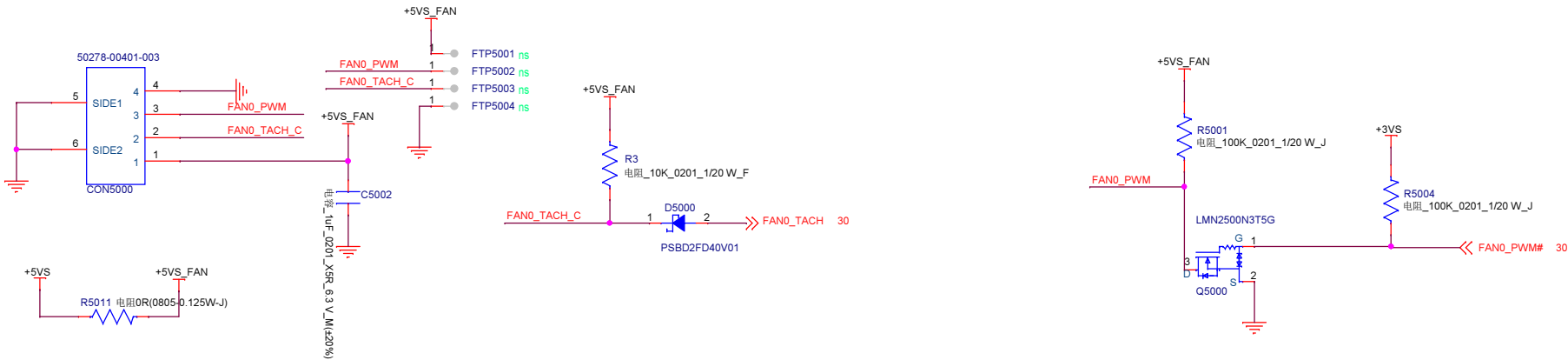




Thermal Sensor for package test

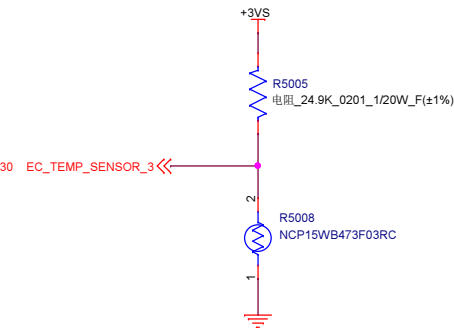


FAN

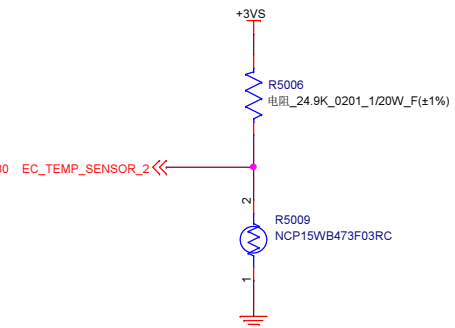


DPTF

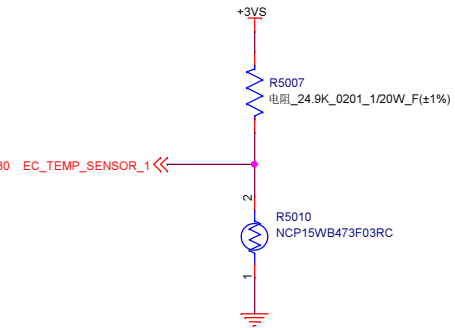
close to CPU VR



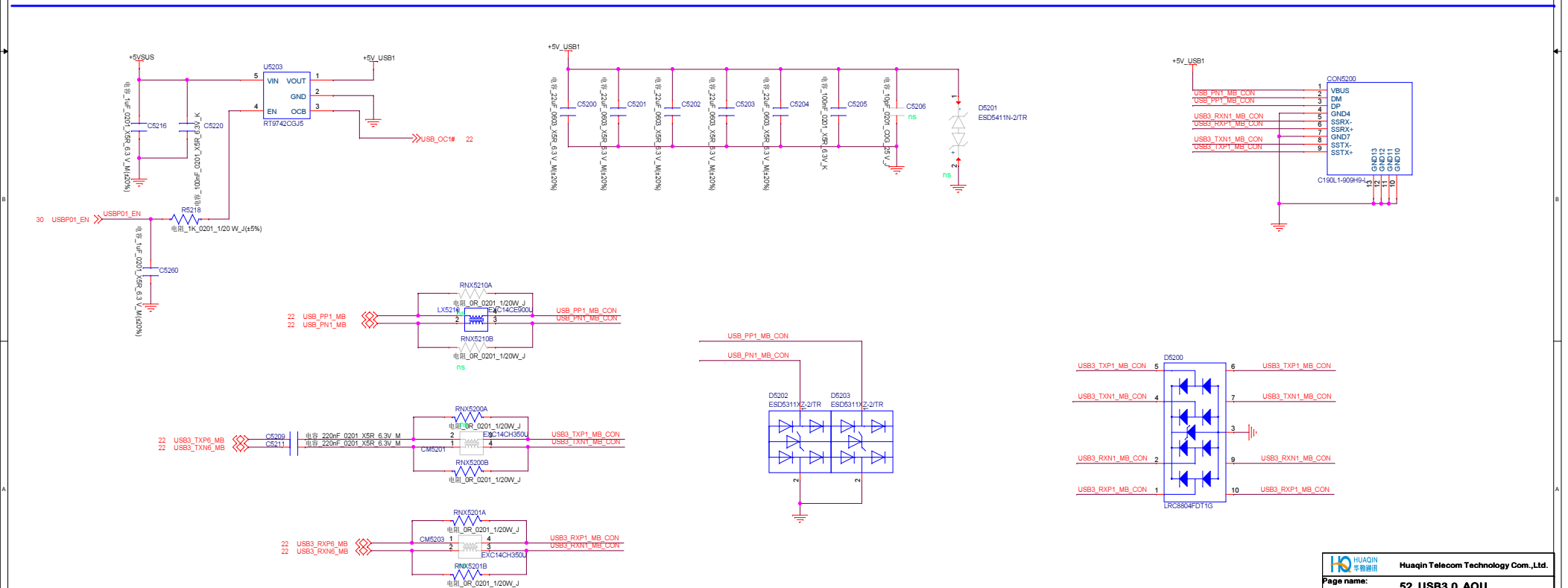
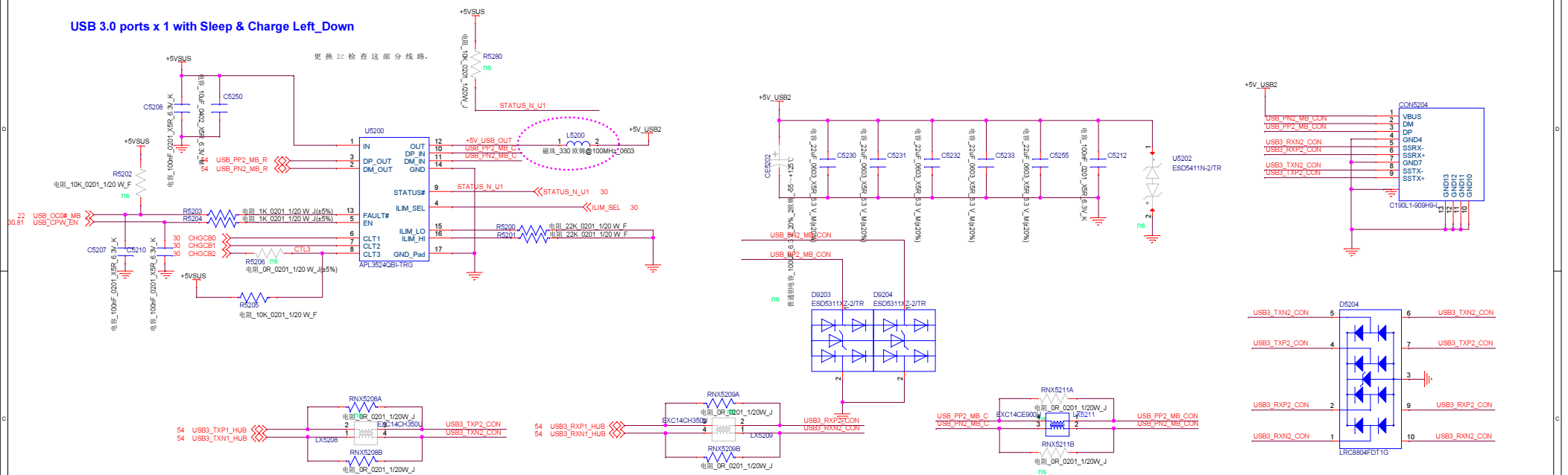
close to GPU VR

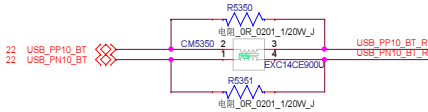
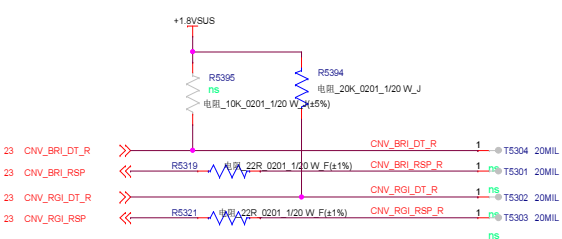
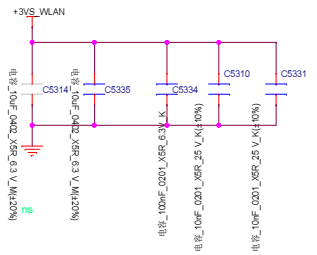
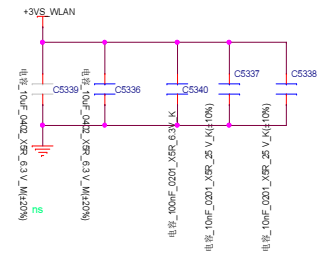
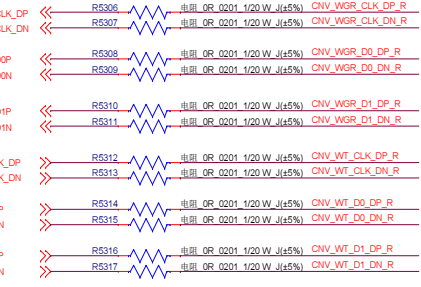
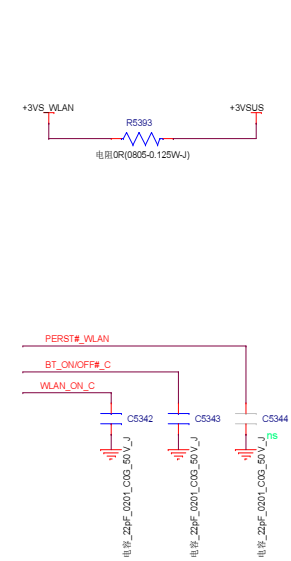


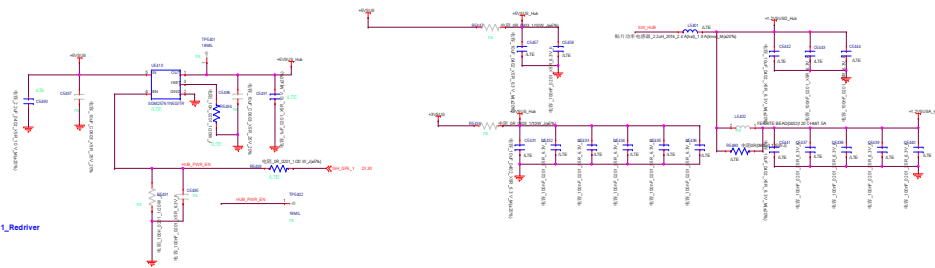
close to RAM



USB 3.0 ports x 1 with Sleep & Charge Left_Down

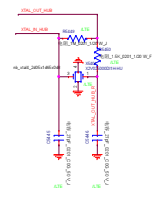
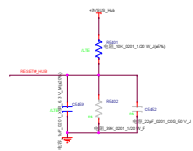
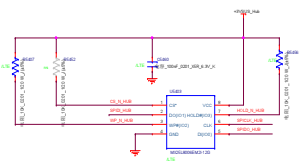
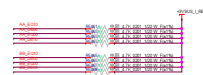
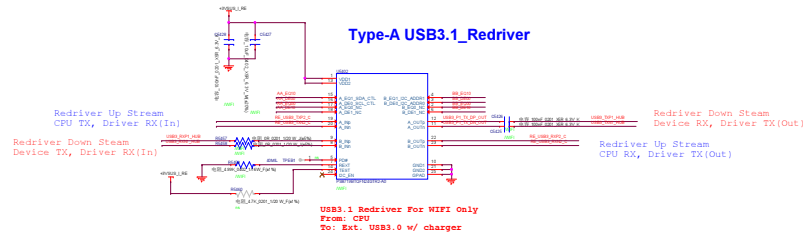
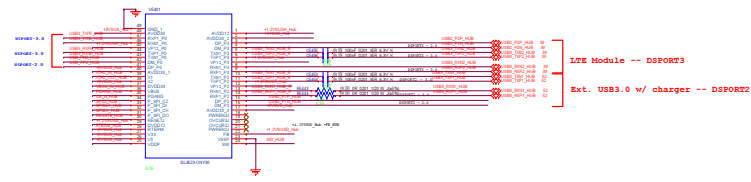


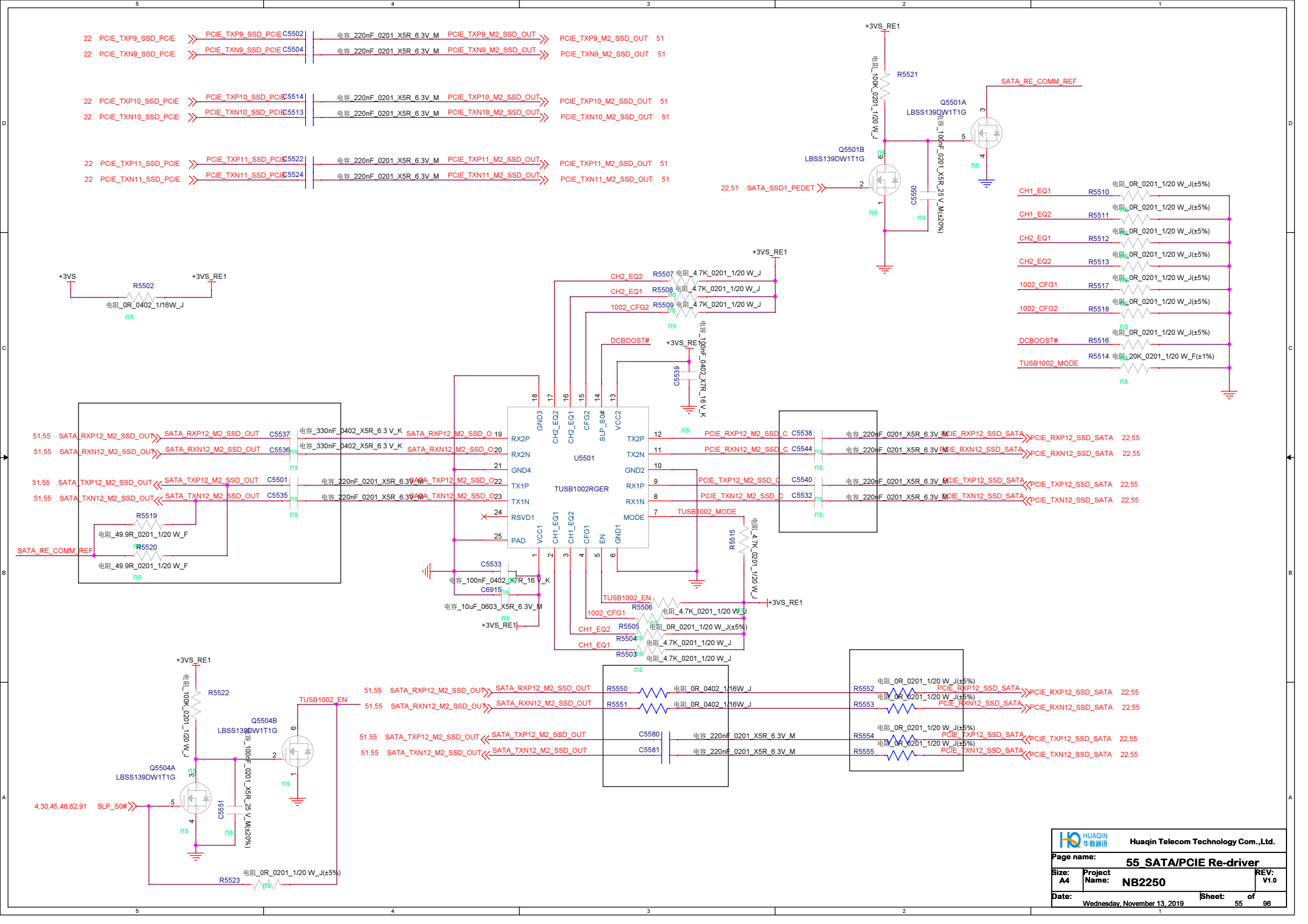


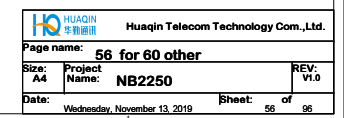


HUB USB Input*1

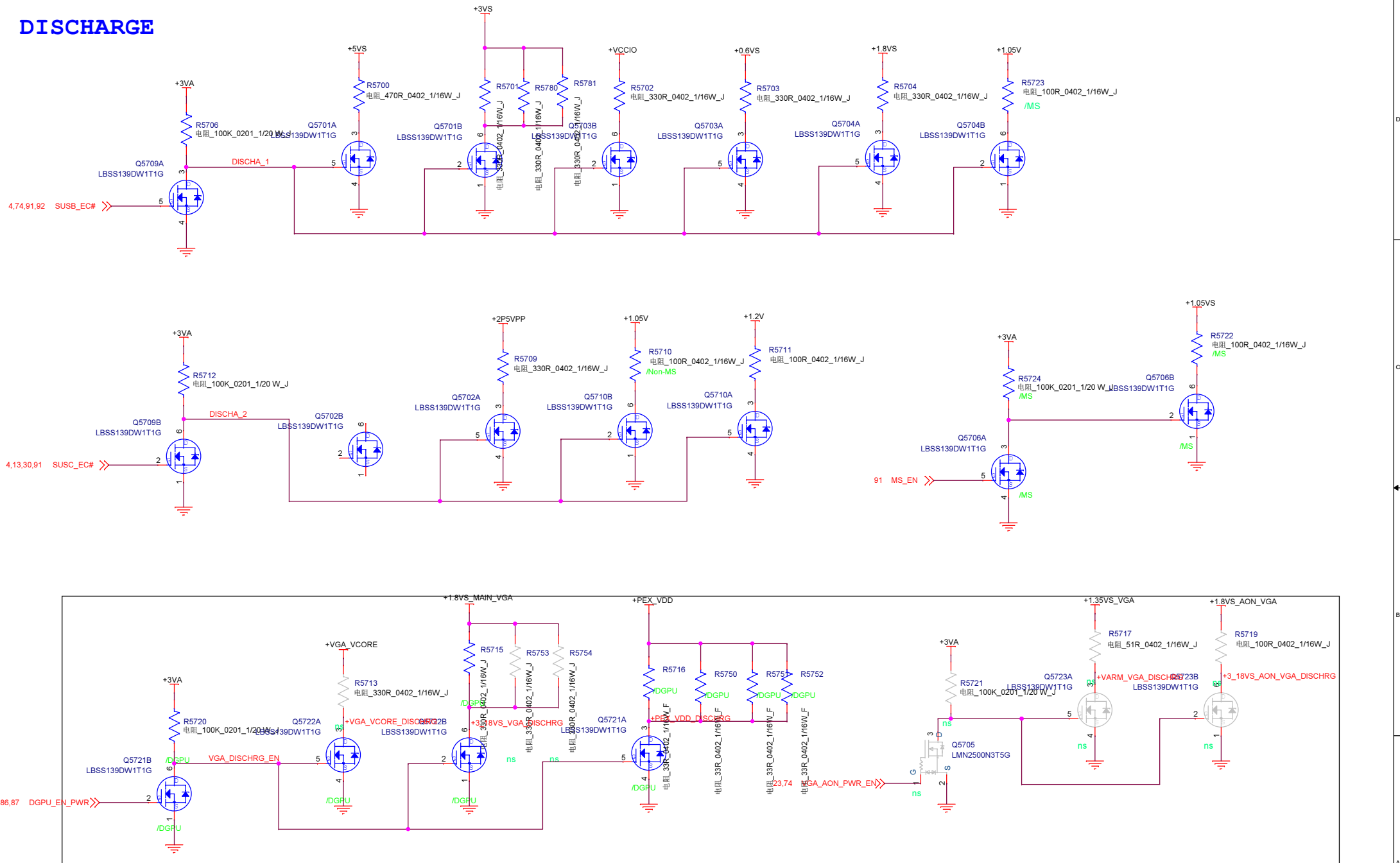
HUB USB Output*2





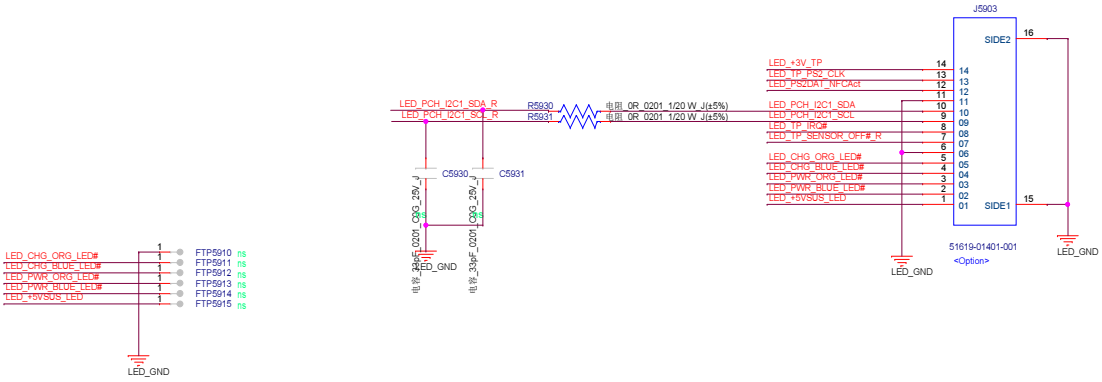


DISCHARGE

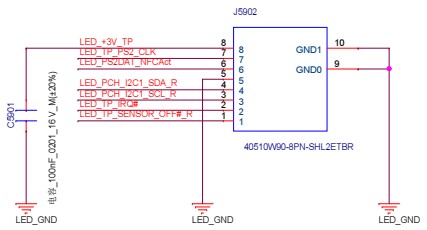




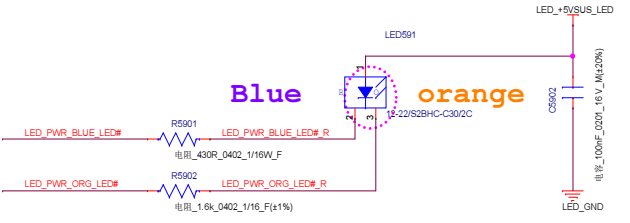
P6 LED Sub Board



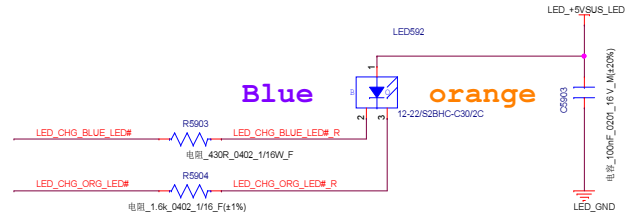
to Click Pad



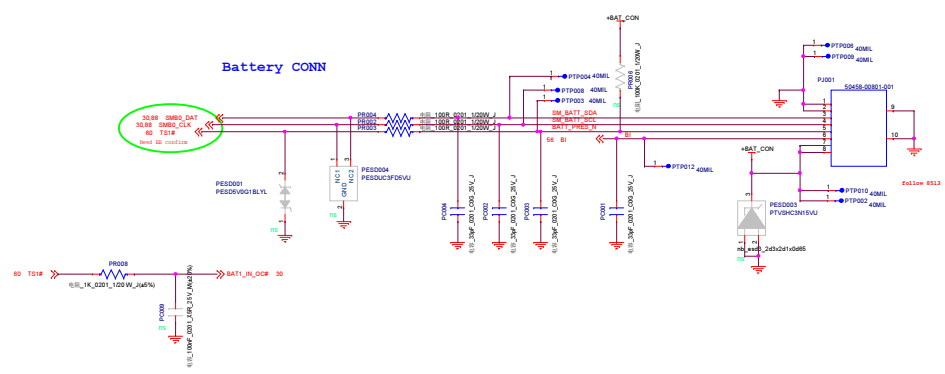
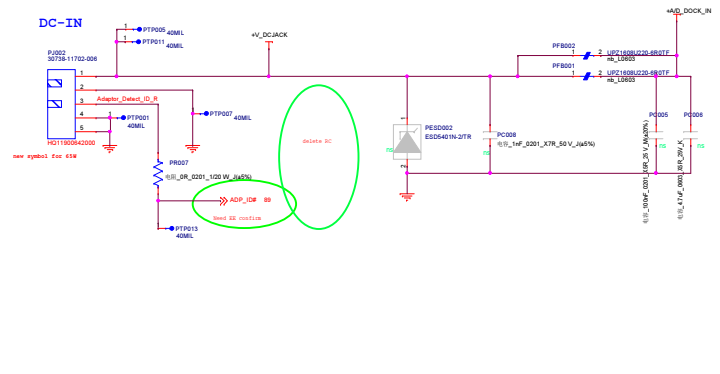
Power LED

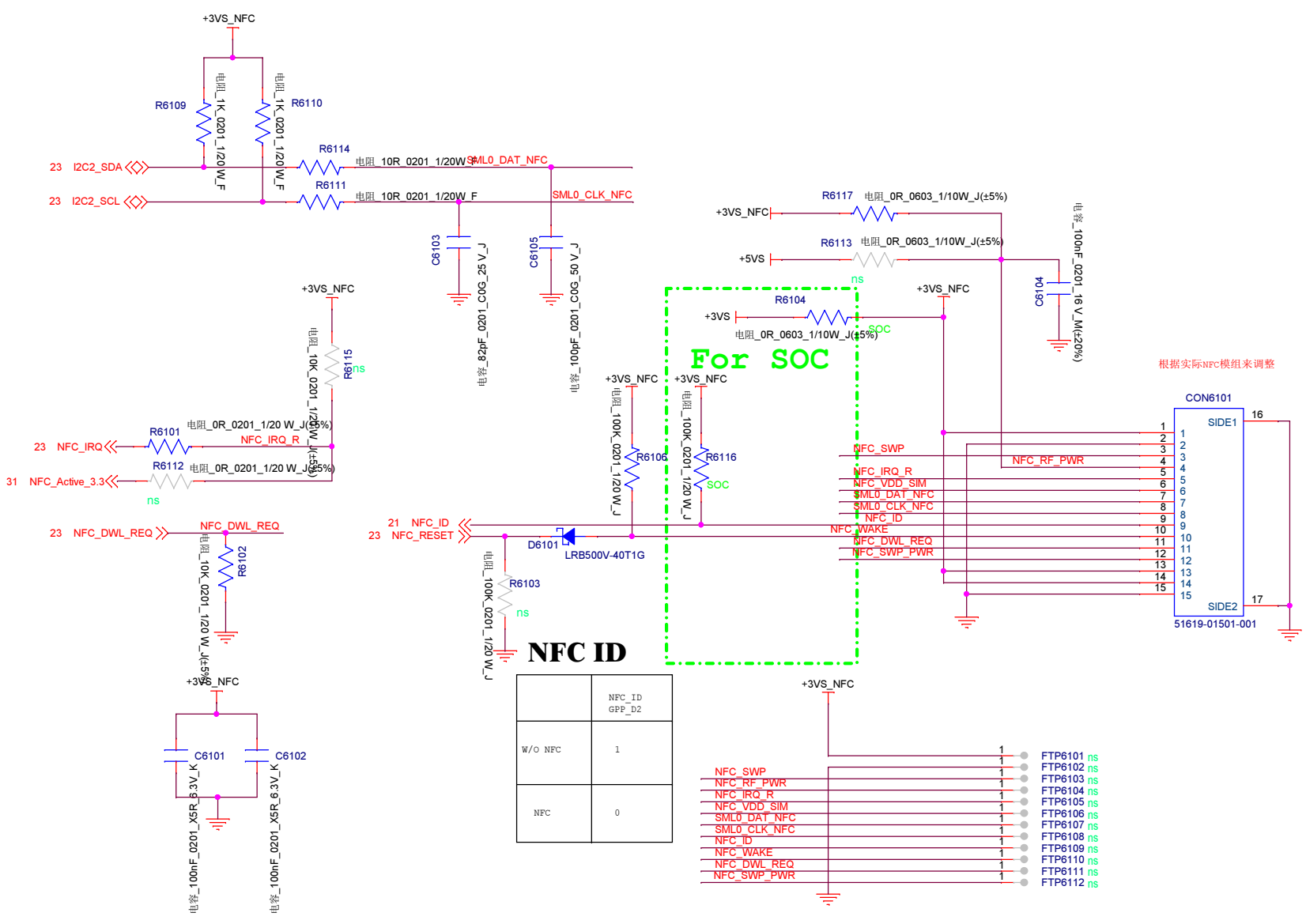


Charger LED



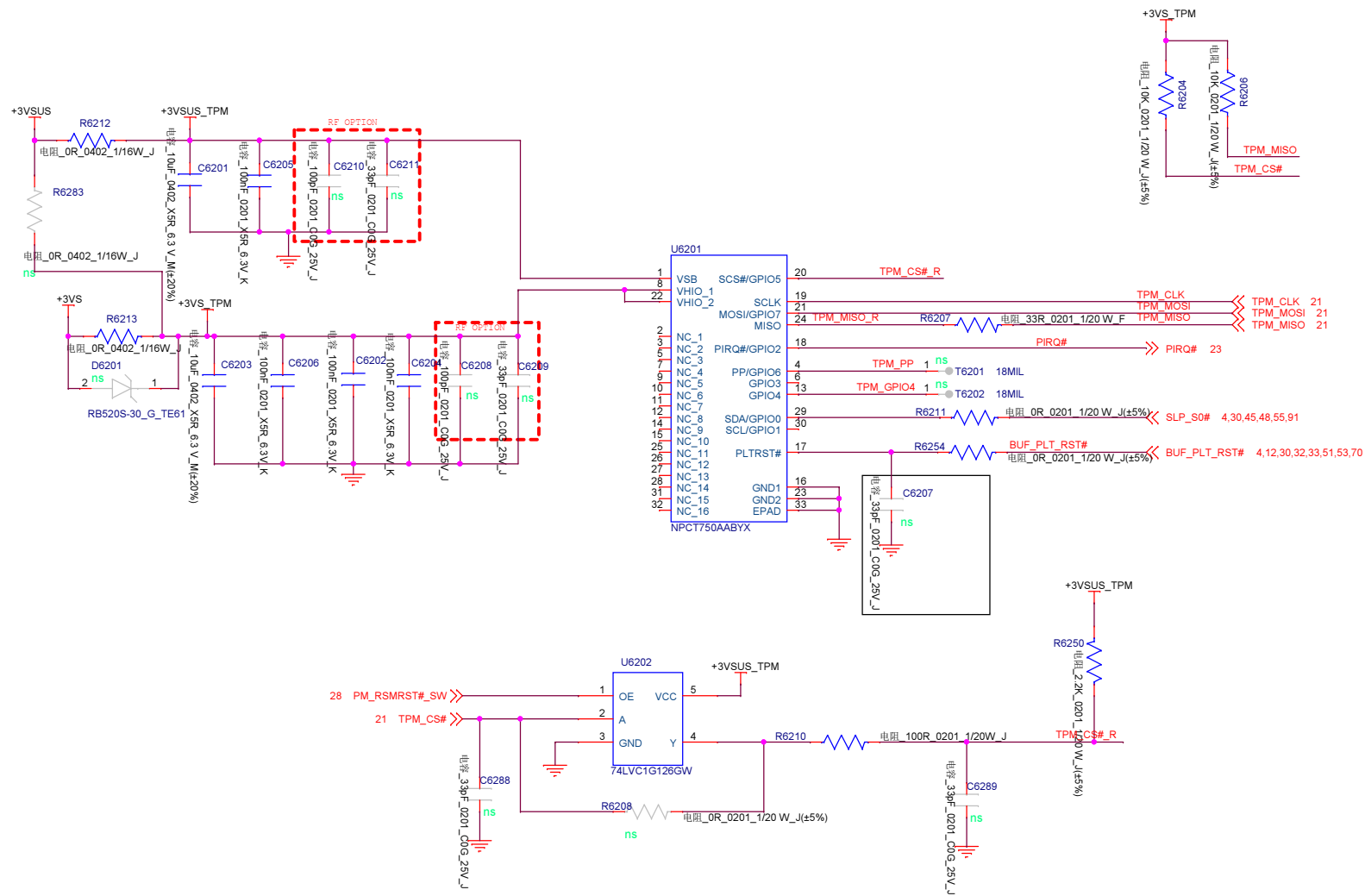
change1_4





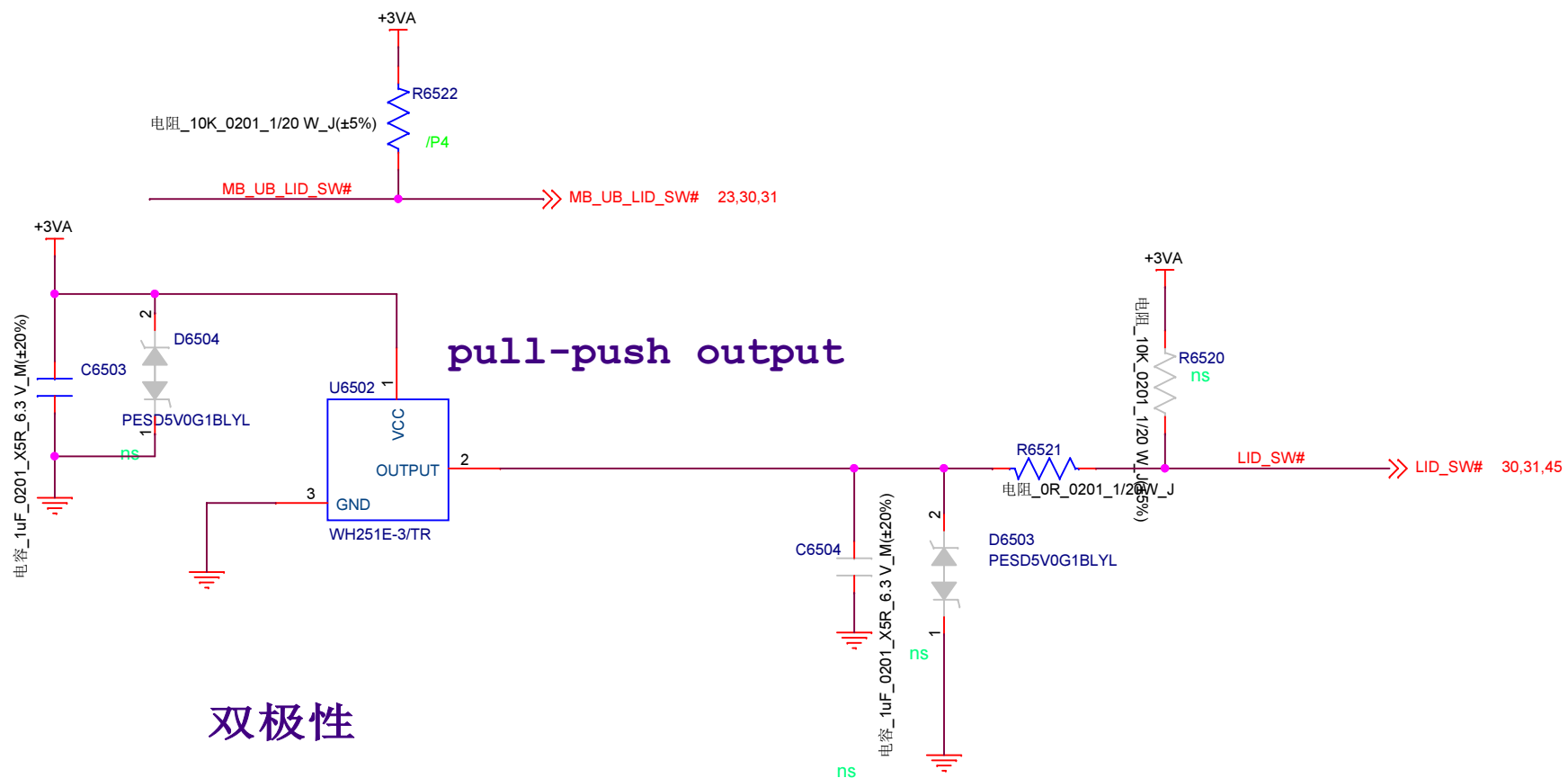
NFC ID

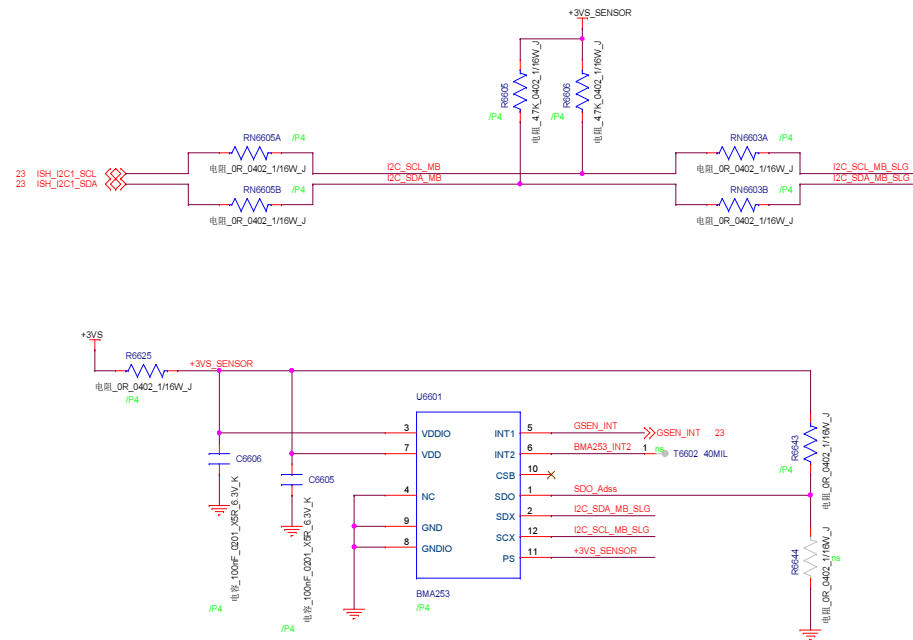
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W/O NFC	1
NFC	0



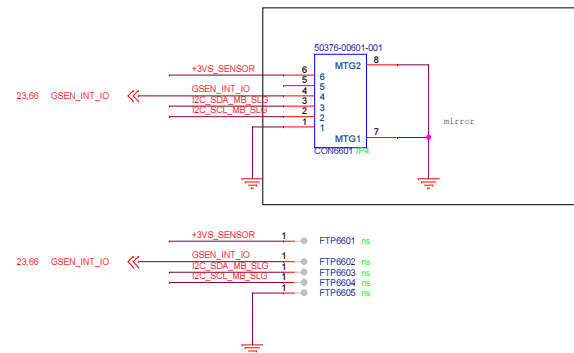






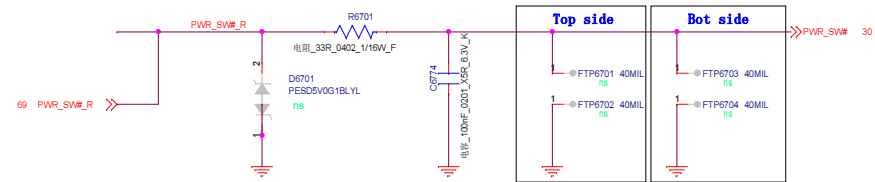
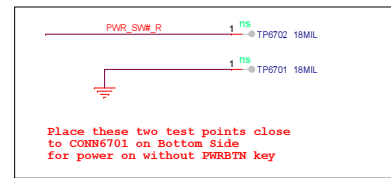
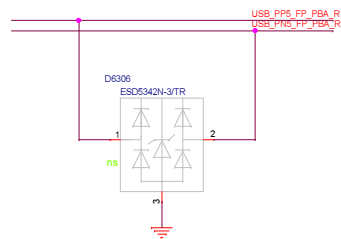
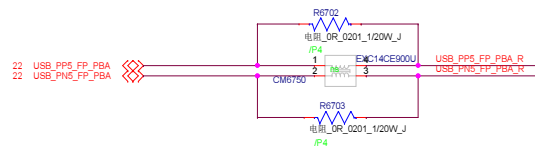
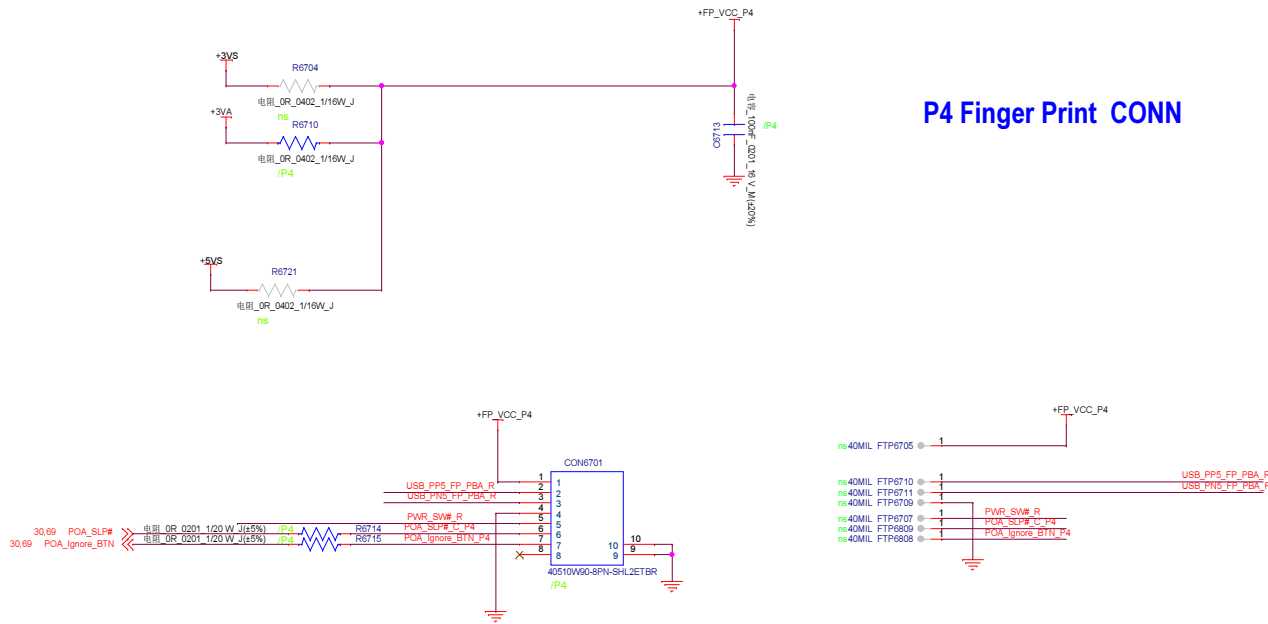


IO side G-Sensor



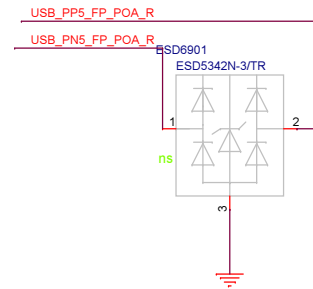
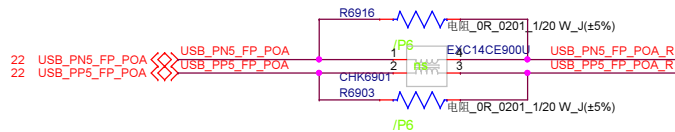
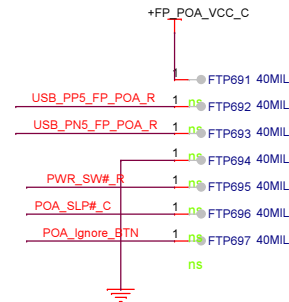
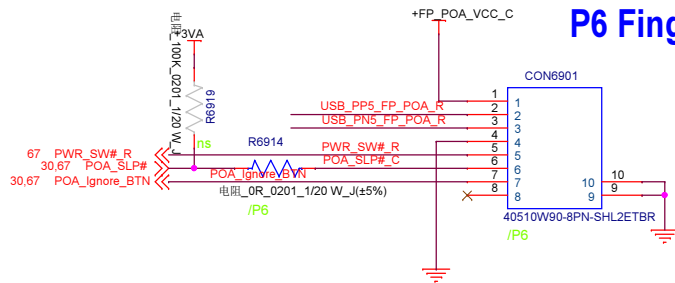
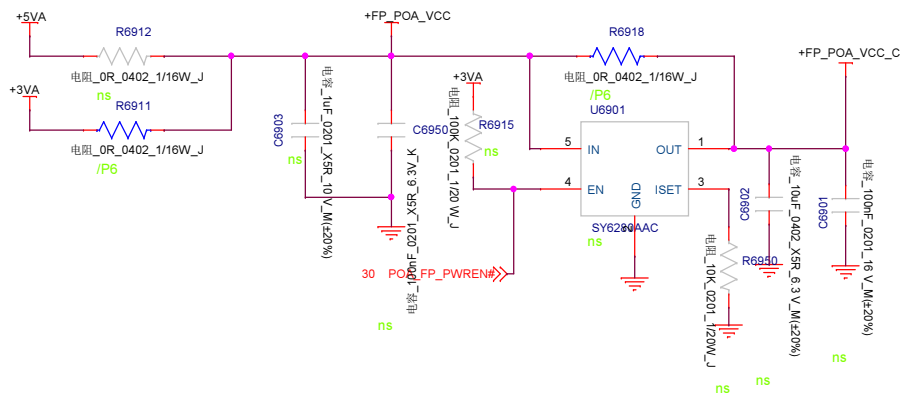
Finger printer

P4 Finger Print CONN





Finger Printer





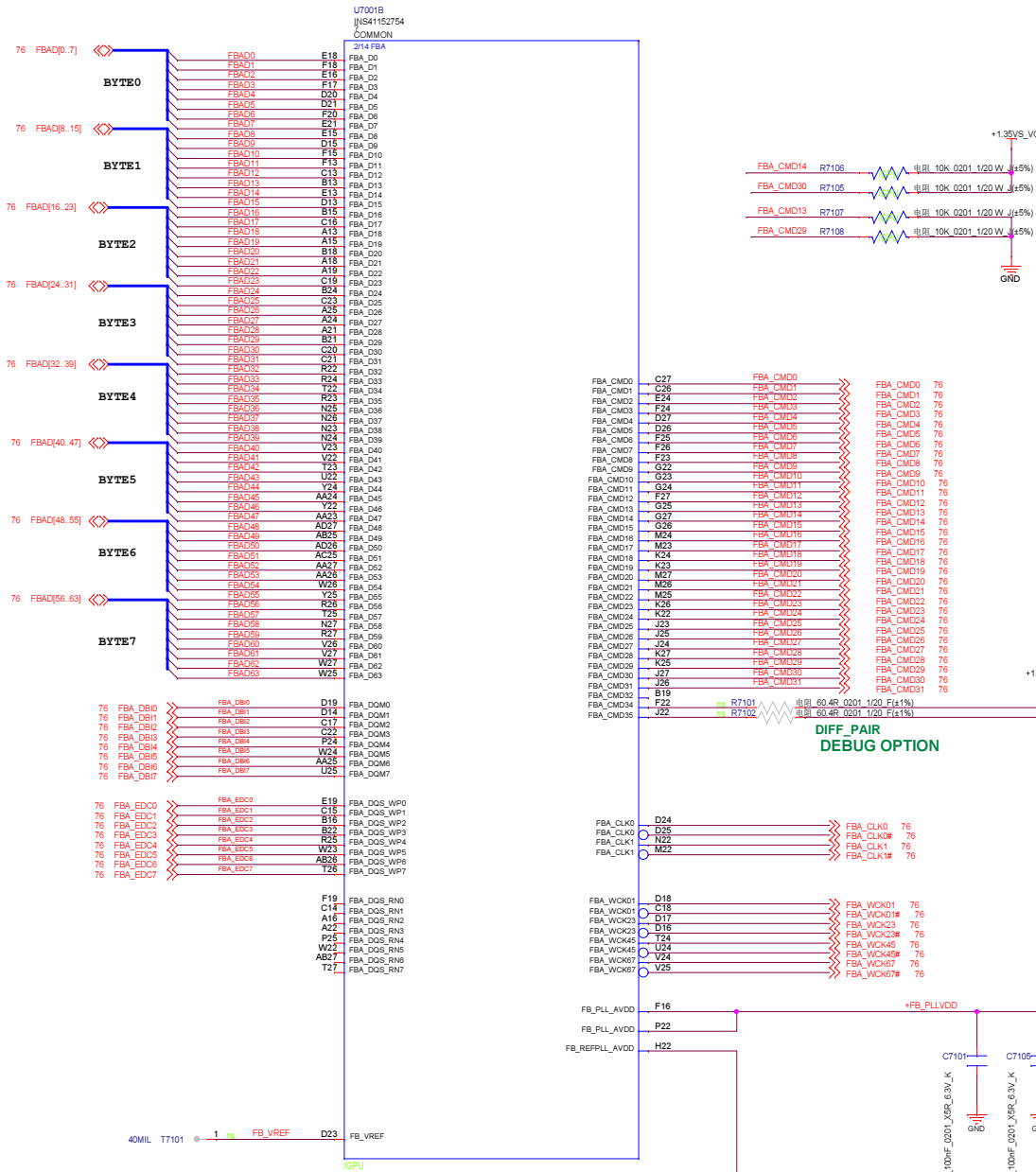
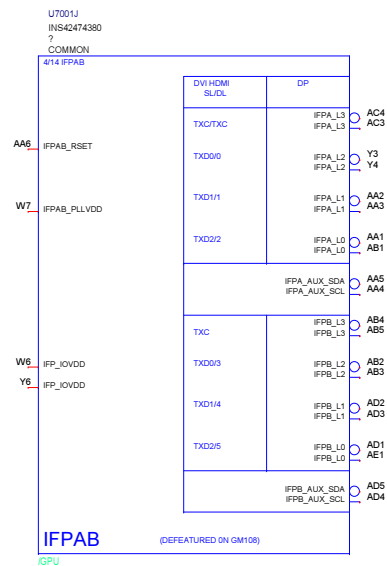


Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB28-64, GB48-128	Channel 0 0..31	GB2-64, GB28-64, GB48-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB28-64, GB48-128 Channel 0 & 1			
CMD32	Hot used		
CMD33 ¹	Hot used		
CMD34	DEBUG0 ²		
CMD35	DEBUG1 ²		

Notes:
1. Hot available in GB2-64 and GB28-64 packages.
2. GPU debug pins; not connected to DRAM. See section 7.1.13.



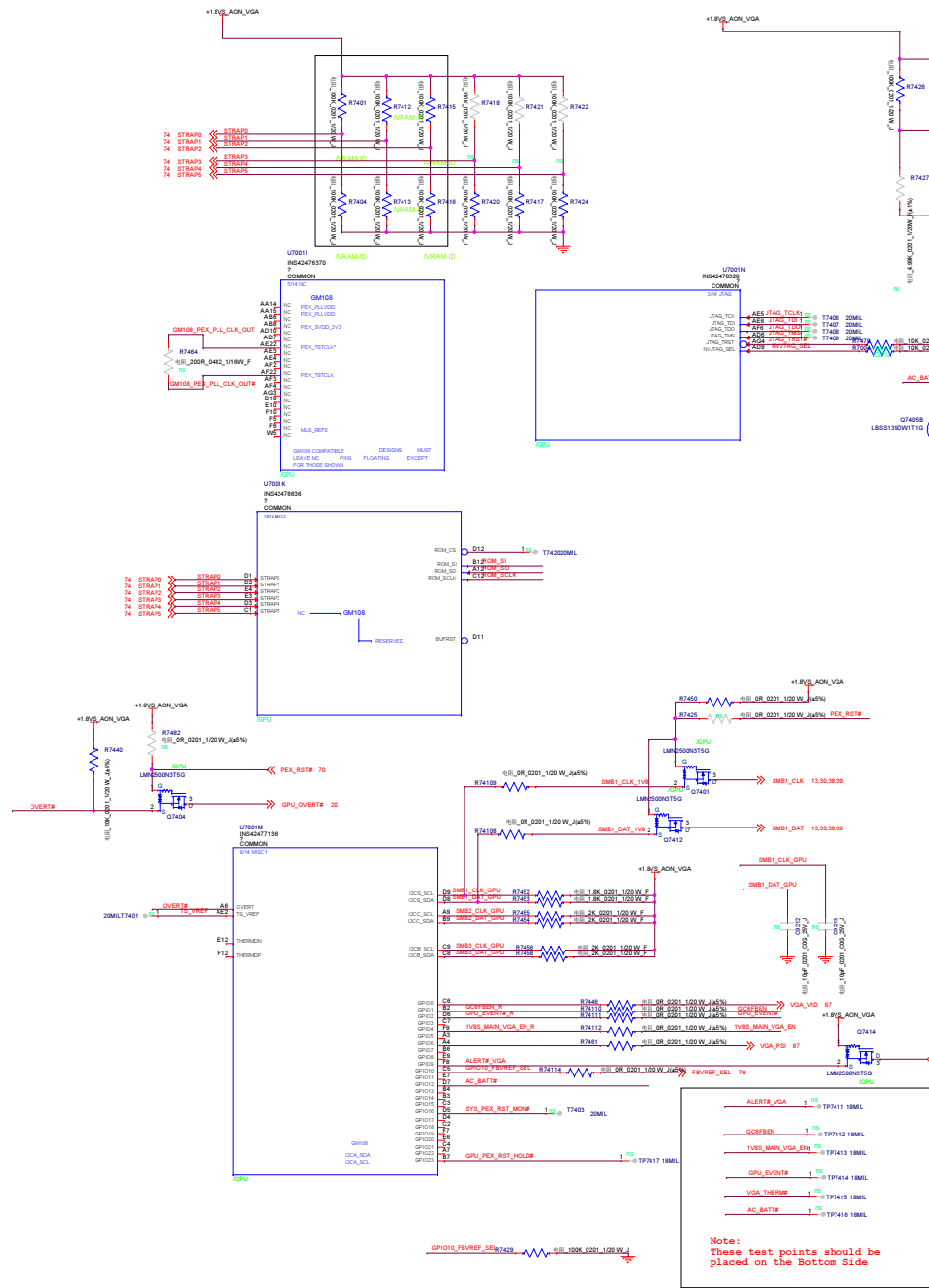
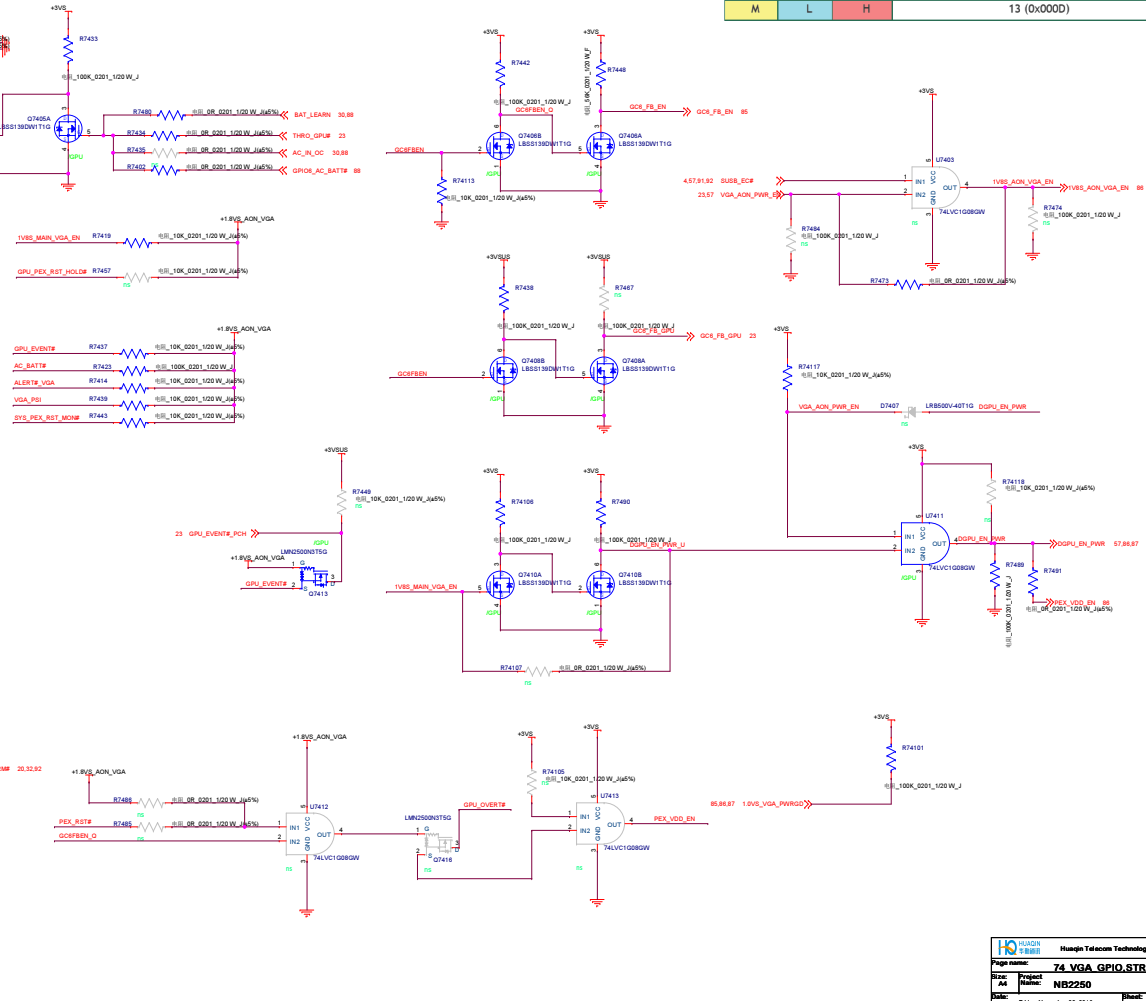


Table 5. N175-G0/G2 DDR5 Recommended Memories

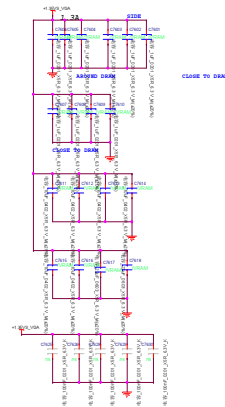
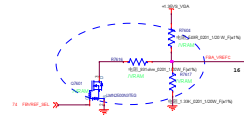
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Hynix	H5GCBH24JR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
M	L	L	11 (0x000B)	
M	L	H	12 (0x000C)	
M	L	M	13 (0x000D)	



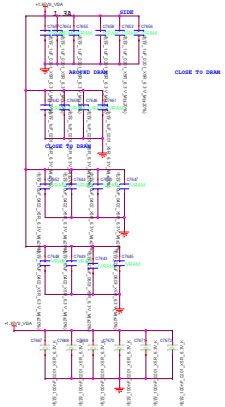
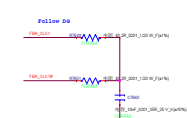
Note:
These test points should be placed on the Bottom Side



This detailed schematic illustrates the internal architecture of the CPU core. It shows the interconnections between numerous functional blocks:

- Instruction Path:** Includes the Instruction Cache (ICACHE), Instruction Decoder (IDCODEC), Branch Predictor (BRANCHPREDICTOR), and Instruction Queue (INSTRQ).
- Execution Units:** Features multiple ALUs (ALU0 through ALU7) and Floating-Point Units (FPU0 through FPU7).
- Register File:** A central component containing registers R0 through R31.
- Control Logic:** Includes the Program Counter (PC), Branch Target Address (BTARGET), and various control signals like BRANCH, JUMP, and RET.
- Data Paths:** Shows the flow of data between registers, ALUs, and memory units, including the Data Cache (DCACHE) and Memory Controller (MEMCONTROLLER).

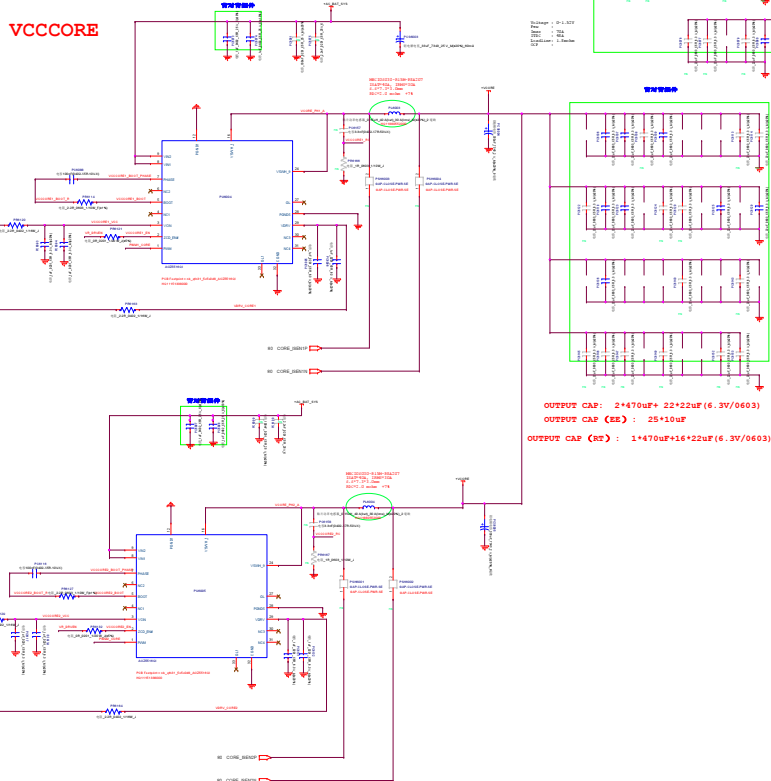
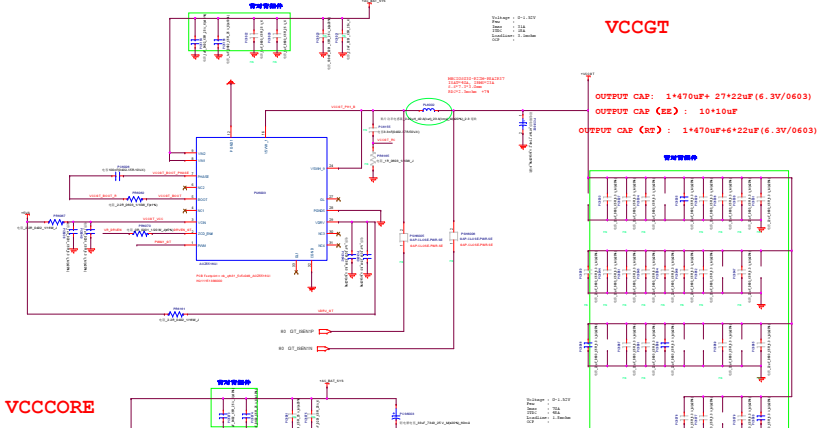
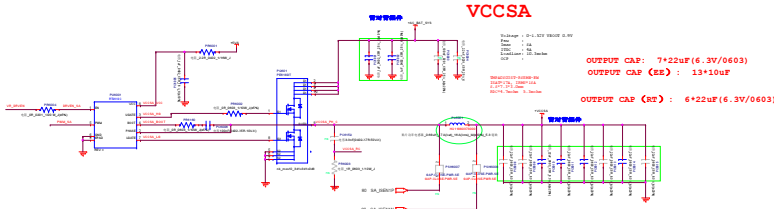
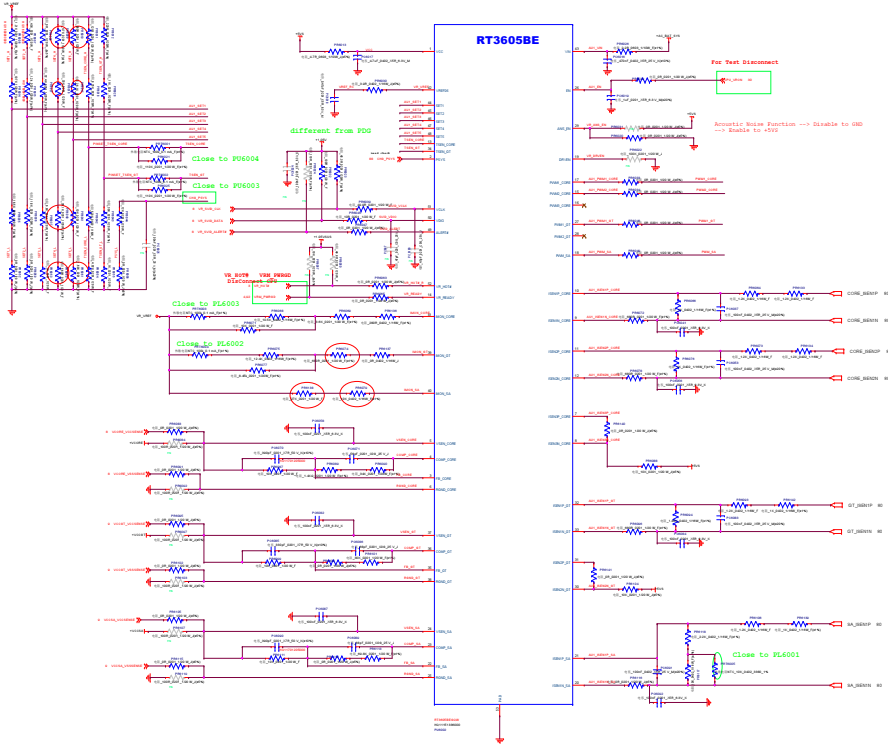
The diagram uses color-coded buses and labels to represent different types of signals and data paths, providing a comprehensive view of the processor's internal state and connectivity.



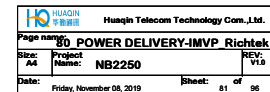
5					4					3					2					1				
D																								
C																								
B																								
A																								



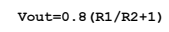
change1 9



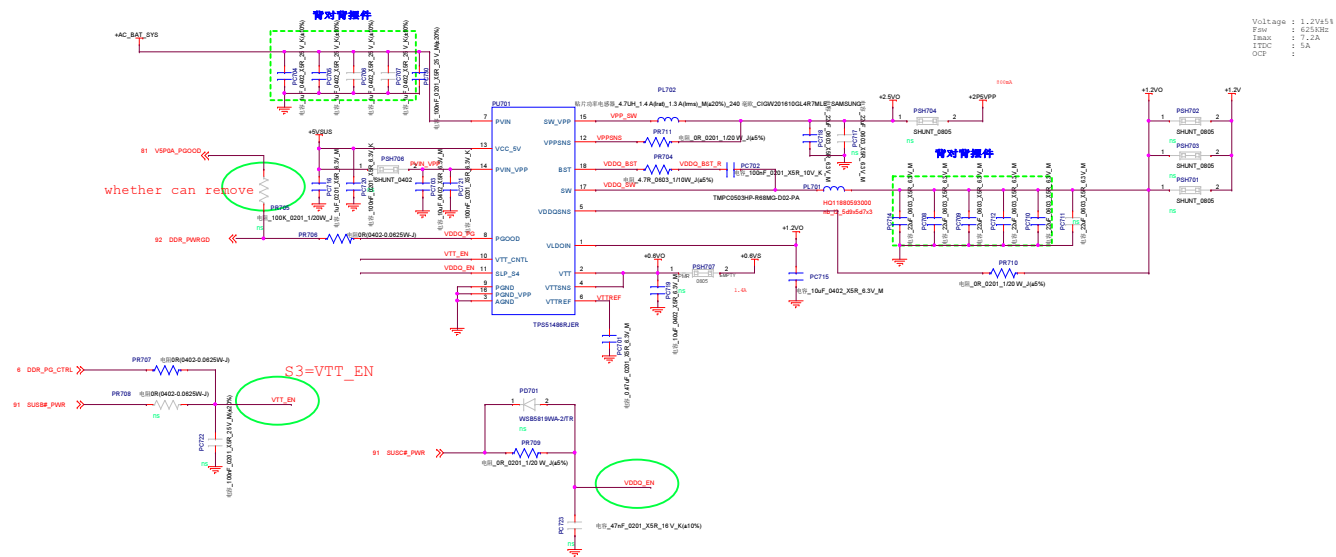
+V3P3A



```
Voltage : 1.05V±5%
Fsw      : 625KHz
Imax     : 9.4A
ITDC     : 3.75A
OCP      :
```



change1_9

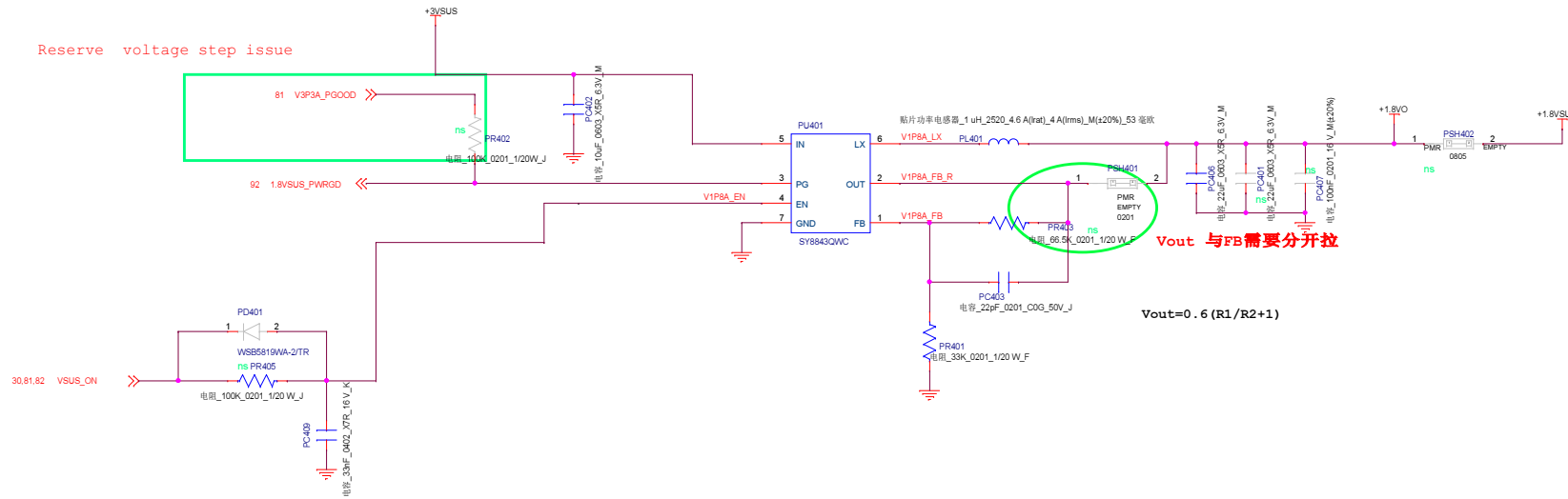


change1_9

+V1P8A

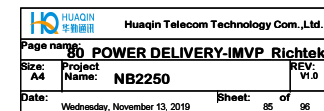
Reserve voltage step issue

```
Voltage : 3.3V±5%
Fsw      : 625KHz
Imax     : 1A
ITDC     :
OCP      :
```


$$V_{out} = 0.6 (R1/R2 + 1)$$

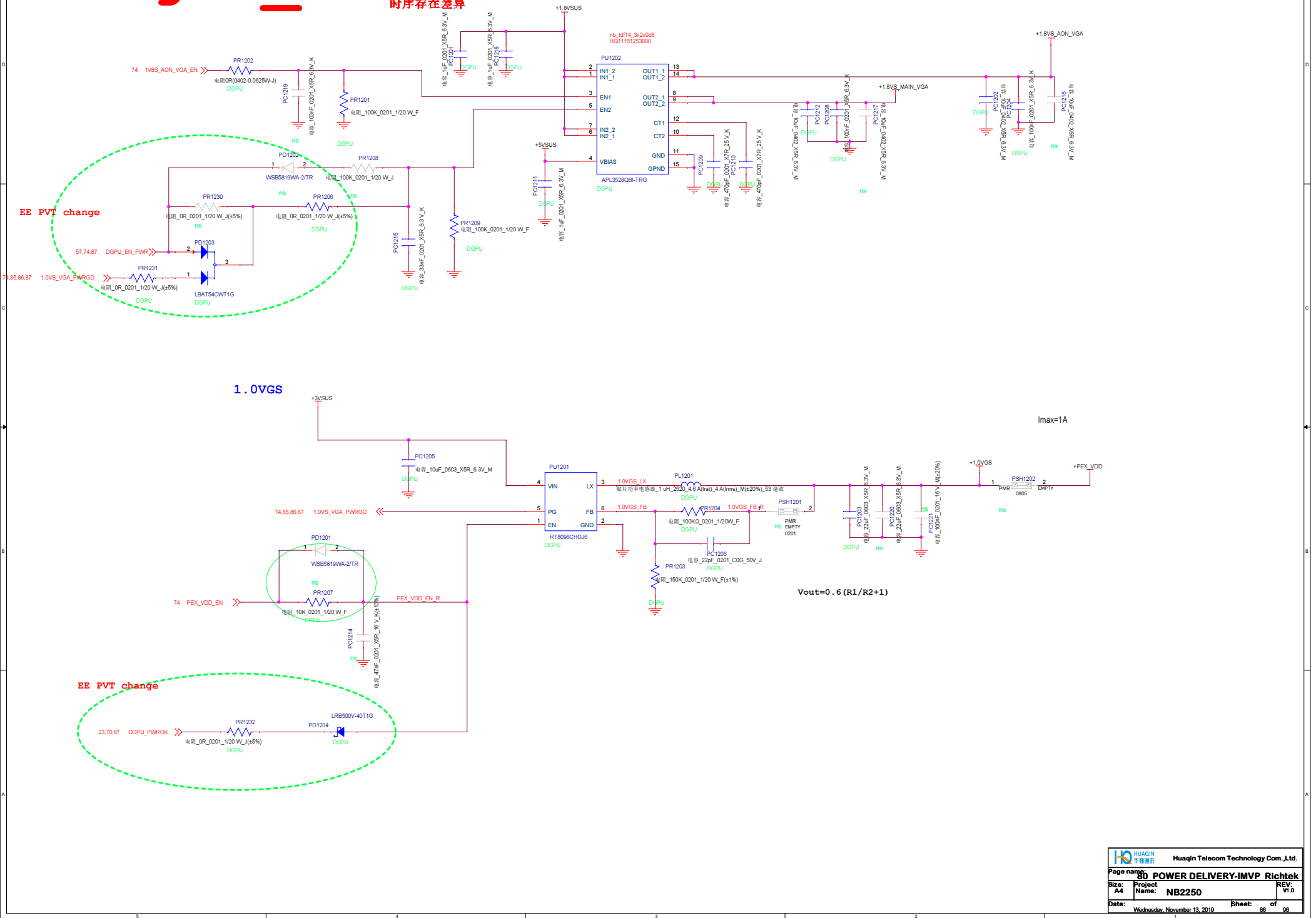
Vout 与FB需要分开拉

```
Voltage : 1.35V±5%
Fsw      : 400KHz
Imax     : 9A
ITDC     : 9A
OCP      :
```



change1_9

时序存在差异



change1_9

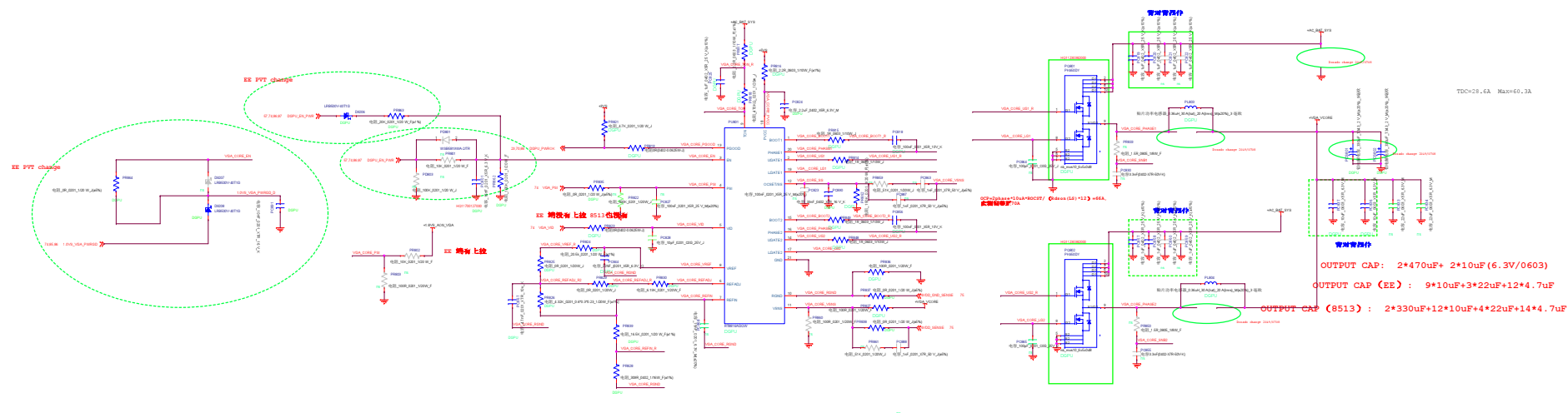
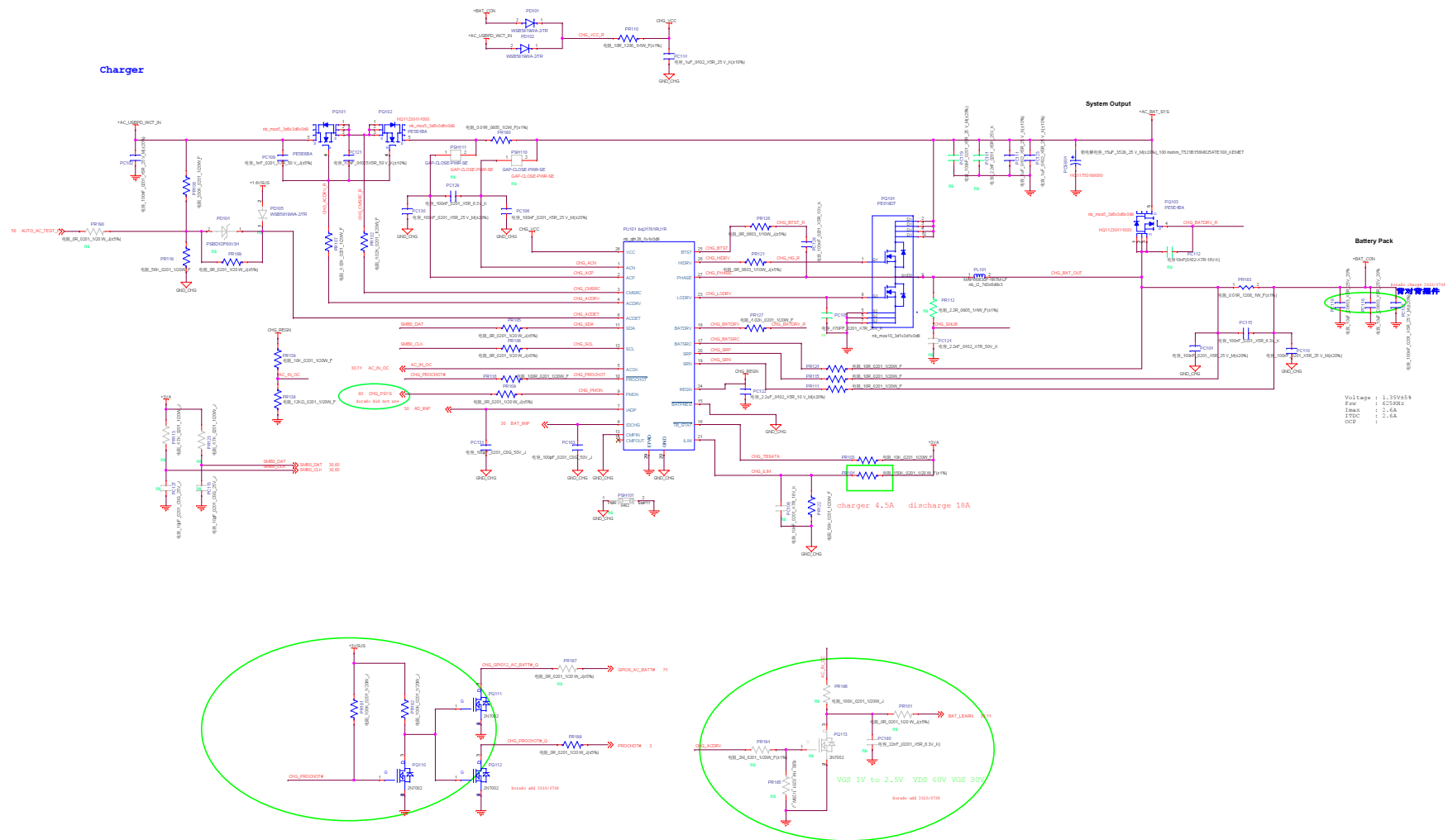


Table 7. Output EDP-Continuous

	NVVD	GPU FBIO	FB Total ¹	1.0V Total ¹	1.8V Total ²
Product	(A)	(A)	(A)	(A)	(A)
N175-LG	15.4	2.5	5.0	0.1	0.2
N175-G1	30.0	3.0	5.6	0.1	0.3
N175-G0 ⁶	27.8	3.2	5.8	0.2	0.5
N175-G2 ⁶	28.6	3.2	5.8	0.2	0.5

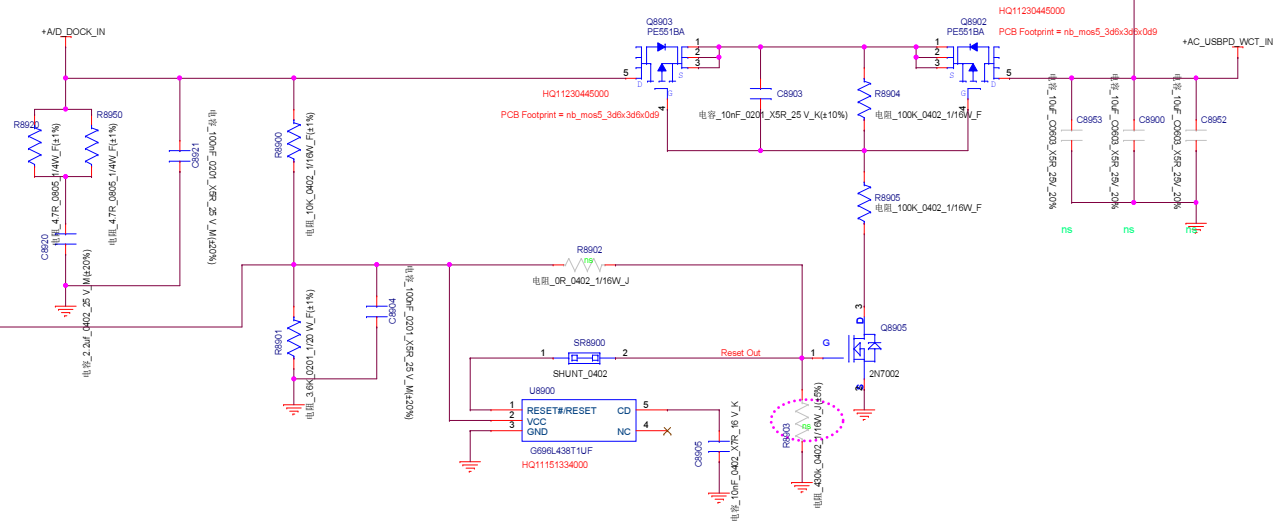
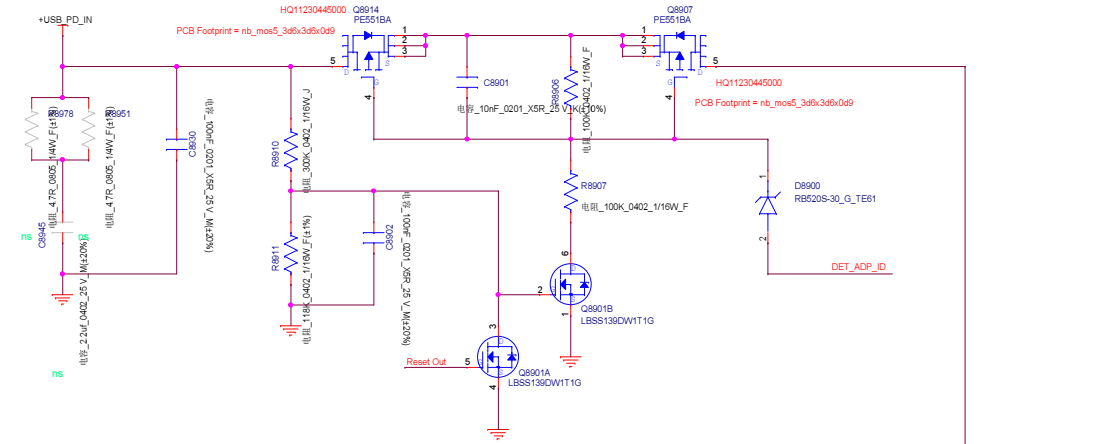
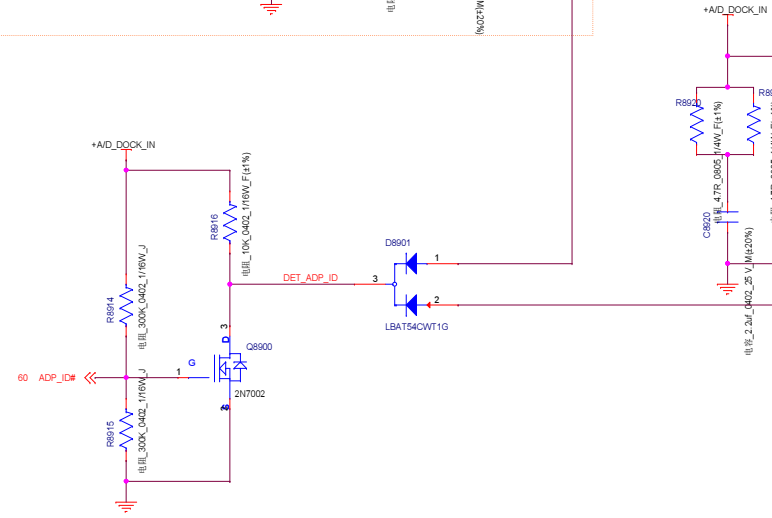
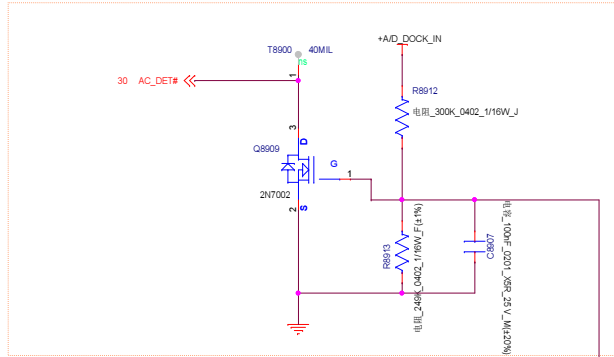
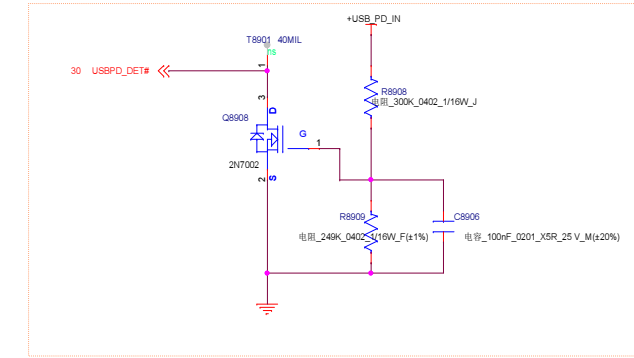
Table 8. Output EDP-Peak

	NVVD	GPU FBIO	FB TOTAL ⁴	1.0V Total ¹
	—	1.35V ³	1.35V ³	1.0V ³
Product	(A)	(A)	(A)	(A)
N175-LG	48.3	2.8	5.8	0.2
N175-G1	60.1	3.4	6.9	0.2
N175-G0 ⁵	42.0	3.9	7.4	0.3
N175-G2 ⁵	60.3	3.9	7.4	0.3



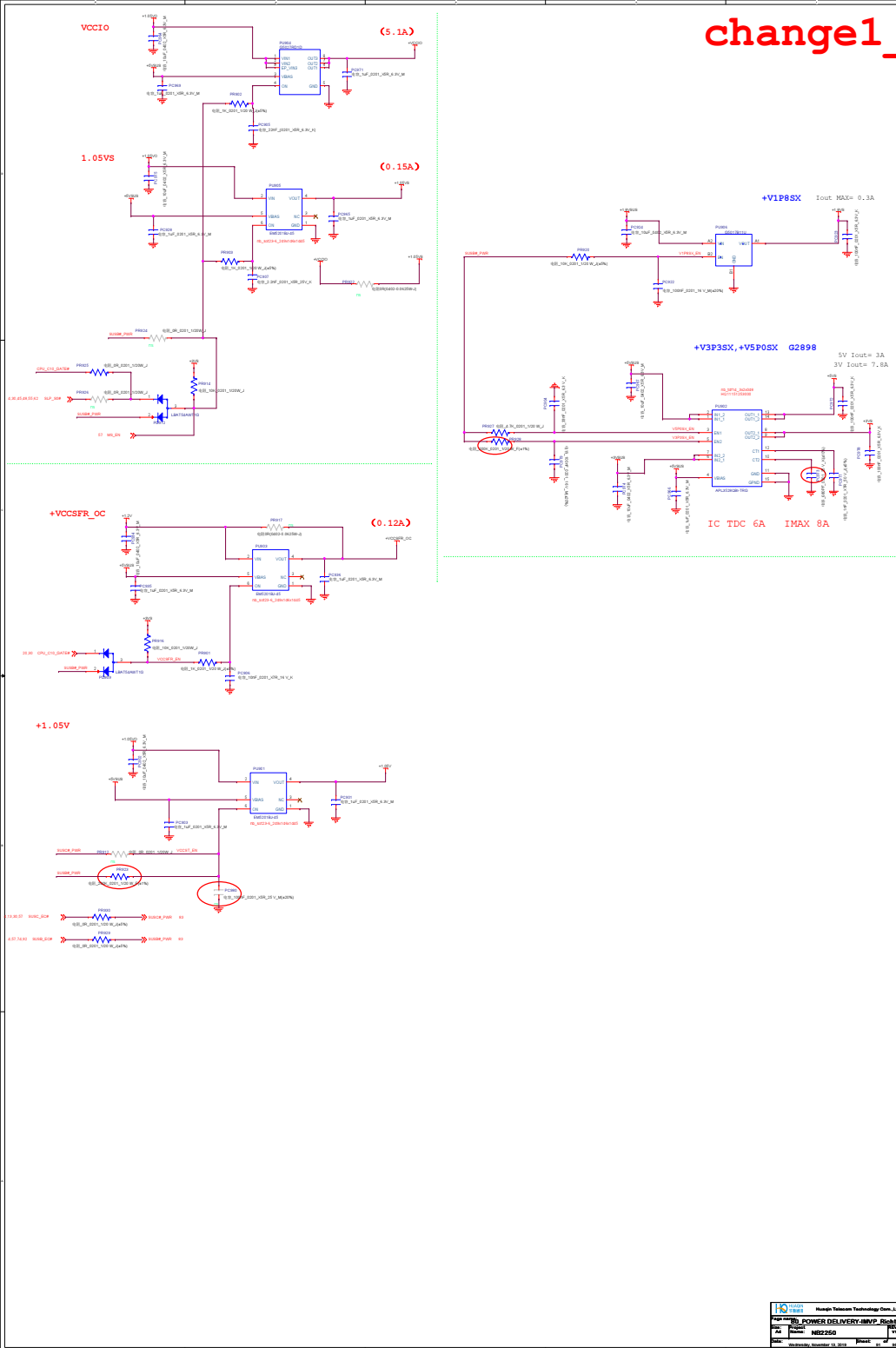
AC & USB_PD Detect

2 Input switch Circuit

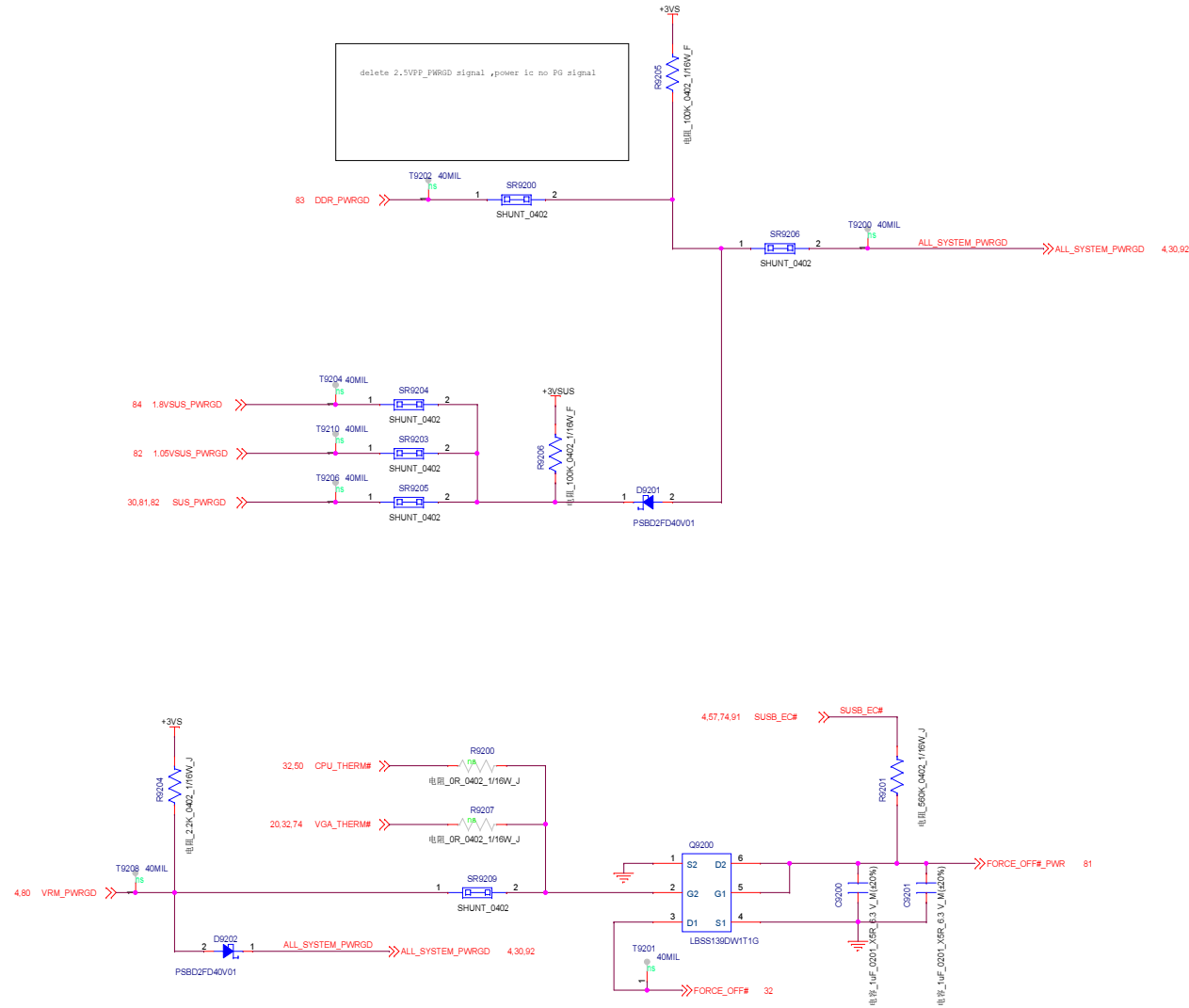




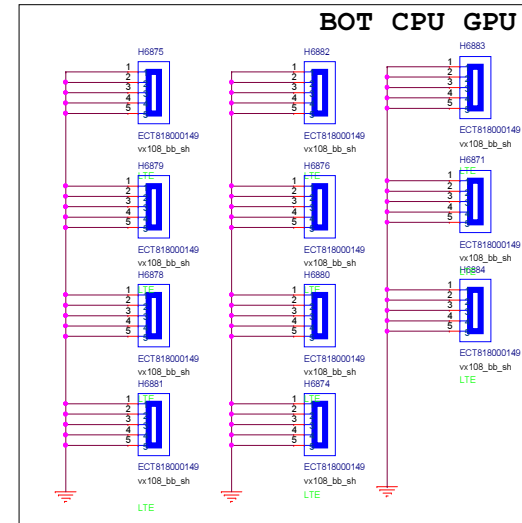
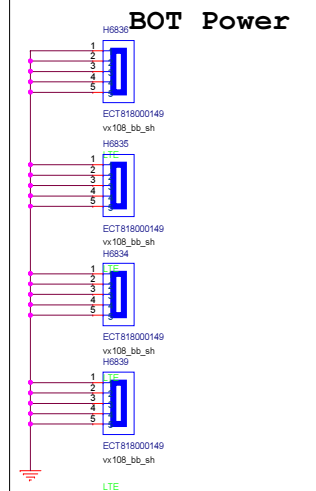
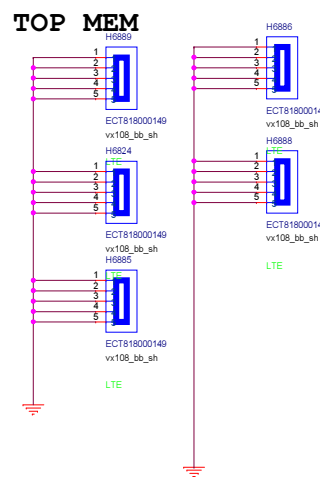
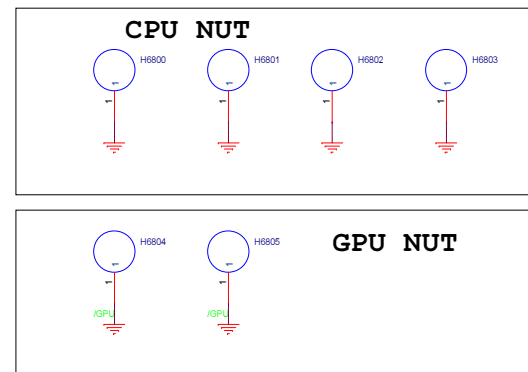
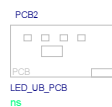
change1_9



POWER GOOD DETECTOR







change1_9

